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Low-Power CMOS image sensor with multi-column-parallel SAR ADC

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Abstract

This work presents a low-power CMOS image sensor (CIS) with a multi-column-parallel (MCP) readout structure while focusing on improving its performance compared to previous works. A delta readout scheme that utilizes the image characteristics is optimized for the MCP readout structure. By simply alternating the MCP readout direction for each row selection, additional memory for the row-to-row delta readout is not required, resulting in a reduced area of occupation compared to the previous work. In addition, the bias current of a pre-amplifier in a successive approximate register (SAR) analog-to-digital converter (ADC) changes according to the operating period to improve the power efficiency. The prototype CIS chip was fabricated using a 0.18-μm CMOS process. A 160 × 120 pixel array with 4.4 μm pitch was implemented with a 10-bit SAR ADC. The prototype CIS demonstrated a frame rate of 120 fps with a total power consumption of 1.92 mW.

Keywords: CMOS image sensor (CIS), Successive approximate register (SAR), Analog-to-digital converter (ADC), Image property, Delta readout scheme.

1. INTRODUCTION

Currently, customer demands for CMOS image sensor (CIS)-based applications are growing rapidly [1,2]. In particular, multiple CISs are mounted as electronic eyes on personalized portable devices such as mobile phones and healthcare applications. Because such electronic devices are mostly powered by batteries, maintaining low power consumption has become an important design issue for imaging sensor systems.

For analog-to-digital (A/D) conversion of signals, there are various types of readout analog-to-digital converters (ADCs): single-slope (SS) ADC, sigma-delta (∑-Δ) ADC, successive approximate register (SAR) ADC, and cyclic (CY) ADC [3]-[6]. Among them, the SAR ADC has been in the spotlight for low-power readout because it does not consume static power. However, its capacitive digital-to-analog converter (C-DAC) for generating a full A/D reference requires a large area, making it difficult to design a layout in a narrow column pitch. Moreover, because the pixel pitch becomes smaller for high pixel resolution, the same problem is encountered in other types of column-parallel (CP) readout ADCs. Here, the pixel pitch is equal to the column pitch in the CP readout structure. To overcome this disadvantage, multi-column-parallel (MCP) readout structures in which one readout ADC covers several columns have been reported [7-9].

Recently, in addition to the studies on traditional circuit techniques for low-power design, various studies [8-11] utilizing the characteristics of the input signal have been reported to obtain further performance improvement. In a previous work [8], based on the image properties, a delta readout scheme that reads only the signal difference between two adjacent pixels (Δ_{px}) has been proposed for a power-efficient readout with SAR ADCs. After completing the A/D conversion for the previous pixel by utilizing its most significant bits (MSBs) MSB information, the C-DAC of the SAR ADC is not fully reset; only the remaining least signal bits (LSBs) are reset. MSBs are memorized and then re-switched in C-DAC for the next A/D conversion. Because the MSB information from the previous pixel is highly correlated with a selected pixel, the number of conversion steps is effectively reduced, resulting in a low-power readout.

In this work, with the same motivations as previous studies, we propose a more optimized delta readout algorithm for rolling-shutter readout CISs adopting the MCP readout structure. Compared to prior studies [8,9], this work considers the row-to-row correlation when changing the row to readout the pixel information (as in rolling shutter readout mechanism). Furthermore,

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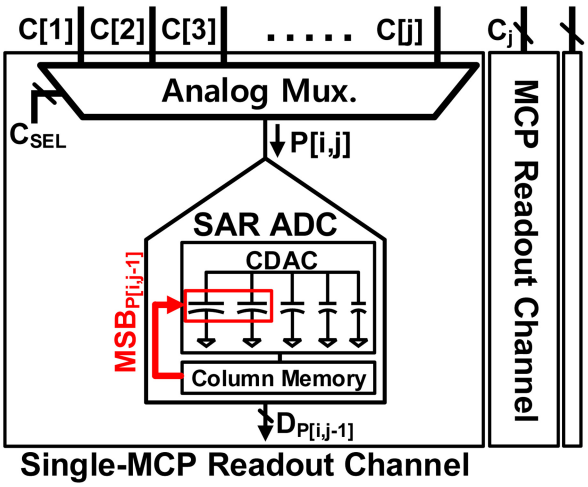

Fig. 1. Multi-column-parallel structure with SAR ADCs.

depending on the readout timings, the power saving effect is maximized by effectively controlling the static bias current of a pre-amplifier in the proposed SAR ADC.

The remainder of this paper is organized as follows: Section 2 describes the circuit design issues of the proposed low-power imaging sensors with an advanced delta readout scheme. The measured results and discussions about the proposed CIS are presented in Section 3, followed by the conclusion in Section 4.

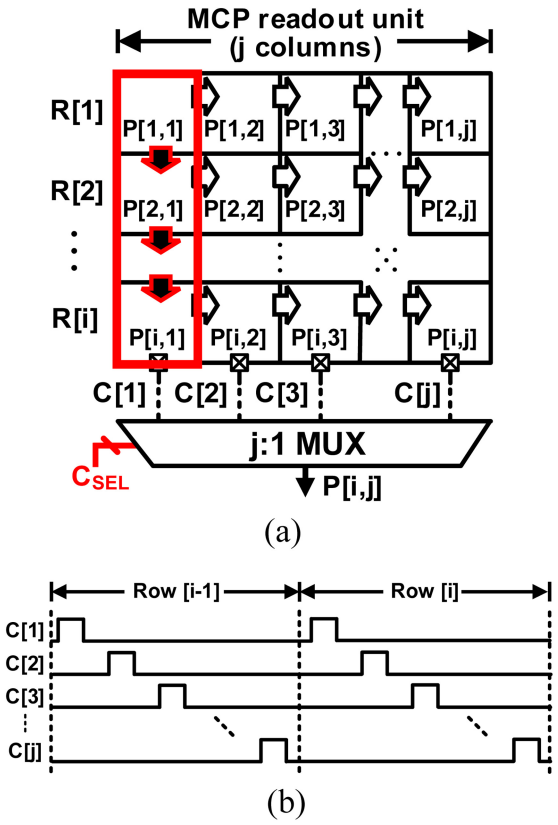

Fig. 2. (a) Explanation of the previously studied delta readout scheme in the row-to-row direction, (b) its MCP readout timing diagram.

2. PROPOSED CMOS IMAGE SENSOR

2.1 Multi-column-parallel readout structure

Fig. 1 shows a simplified schematic of the MCP readout structure [8,12], which uses one readout ADC per multiple columns. The pixel information P[i,j] in each MCP unit of a selected row is sequentially input through the analog MUX to each readout ADC from C[1] to C[j], where i represents the i-th row, and j represents the j-th columns. In this work, the proposed SAR ADC is based on the delta readout scheme similar to that in [8] in which MSBs are copied from the A/D conversion result of the previous pixel ($MSB_{P[i,j-1]}$), and only the remaining LSBs are resolved for the selected pixel.

2.2 Delta Readout Scheme Optimized in MCP readout

The sequence of the delta readout scheme in the MCP readout unit is shown in Fig. 2. There are two readout directions of the column-to-column (P[1,1]→ P[1,j]) and the row-to-row (P[1,1]→ P[i,1]) readout for copying MSBs utilizing the correlation between adjacent pixels. When applying the delta readout in the row-to-row direction, additional memory is required to copy MSBs from the first pixel in the previous row. Although the MCP readout structure is more advantageous in terms of layout design than the CP readout structure, minimizing its area of occupation is still necessary for noise performance and operating speed optimization [7,12]. This issue can be solved by further considering the MCP readout characteristics.

Fig. 3 shows the modified MCP readout direction for the proposed CIS. It is optimized to utilize the correlation between adjacent pixels in the MCP readout structure. Unlike in Fig. 2, each time a row is selected for readout, the analog MUX in the MCP unit changes the selection direction for columns: from C[1] to C[j] in odd rows and from C[j] to C[1] in even rows. In this case, because the delta readout can be applied from P[i-1,j] to P[i,j], no additional memory is required to store the MSB information of P[i,1] in every row.

A simplified schematic of the controller of the analog MUX is

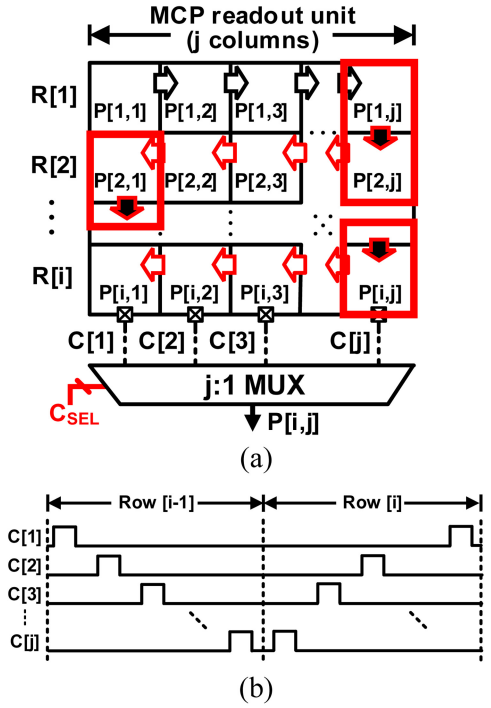

Fig. 3. (a) Modified MCP readout direction for optimizing row-to-row delta readout, (b) its MCP readout timing diagram.

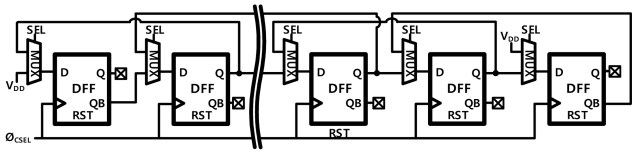

Fig. 4. Simplified schematic of the MCP column selector.

shown in Fig. 4. It is based on the conventional shift register with additional MUXs to change the logical shifting direction depending on the control signal of 'SEL'. The control signals of the analog MUX are globally fed into all MCP readout channels without affecting the circuit performance.

2.3 Bias current controlled readout scheme

Fig. 5 shows a simplified 10-bit SAR ADC applying the delta readout scheme. Similar to [8], the binary-weighted C-DAC is composed of an MSBs-DAC, an LSBs-DAC, and a win-DAC. In this study, a pre-amplifier based on an operational transconductance amplifier (OTA) [13] is used in the comparator as a typical two-stage topology. During A/D conversion, the pre-amplifier minimizes kickback noise and coupling noise in the columns of the MCP unit. However, this leads to high power consumption owing to the use of constant current during the entire CIS

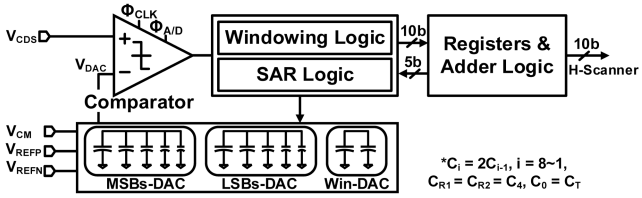

Fig. 5. Simplified schematic of the delta readout SAR ADC.

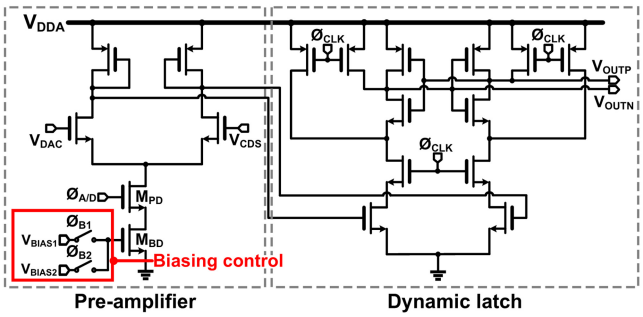

Fig. 6. Simplified schematic of the two-stage comparator.

operation.

Fig. 6 shows a simplified schematic of the designed two-stage comparator of the pre-amplifier stage and the dynamic latch. To minimize the current dissipation, the bias voltage of the M_{BD} in the pre-amplifier is controlled depending on the operation period. The 1-row conversion period (T_{ROW}) is composed of the pixel reset $Ø_{RST}$ and pixel readout $Ø_{SIG}$ period (T_{B1}) and A/D conversion period (T_{B2}). Because a high current is required only during T_{B2}, the proper bias voltage (V_{BAIS2}) is supplied to the M_{BD} to ensure the speed and voltage gain of the pre-amplifier. Then, during T_{B1}, its bias current is lowered by supplying V_{BAIS1}, which changes only the static operating point of the pre-amplifier. This results in a reduction of power consumption. The average current (I_{avg}) of the pre-amplifier can be calculated by

$$I_{avg} = \frac{(I_{B1} \cdot T_{B1} + I_{B2} \cdot T_{B2})}{T_{A/D}}, \quad (1)$$

where I_{B1} and I_{B2} are the currents of the pre-amplifier during T_{B1} and T_{B2}, respectively. In this work, a bias current of approximately 2.55 µA was used during T_{B2} to maximize the performance of the comparator, and in the rest of the operation period T_{B1}, a bias current of approximately 1.55 µA was used to reduce the power consumption.

The overall timing diagram is shown in Fig. 7. During $Ø_{A/D}$, all columns in each MCP unit are sequentially selected, and the A/D conversion is performed. The bias voltages of V_{BAIS1} and V_{BAIS2} for the pre-amplifier are supplied according to the operating

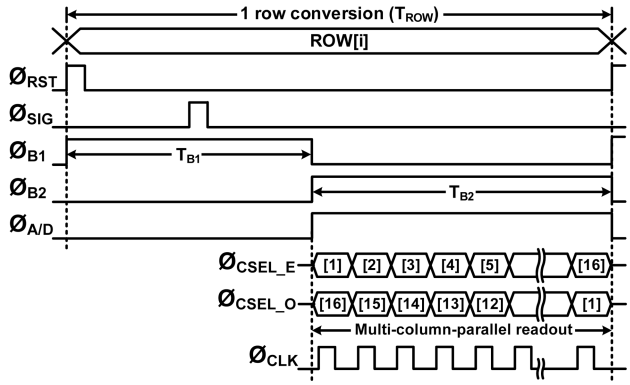

Fig. 7. Overall timing diagram of the prototype CIS.

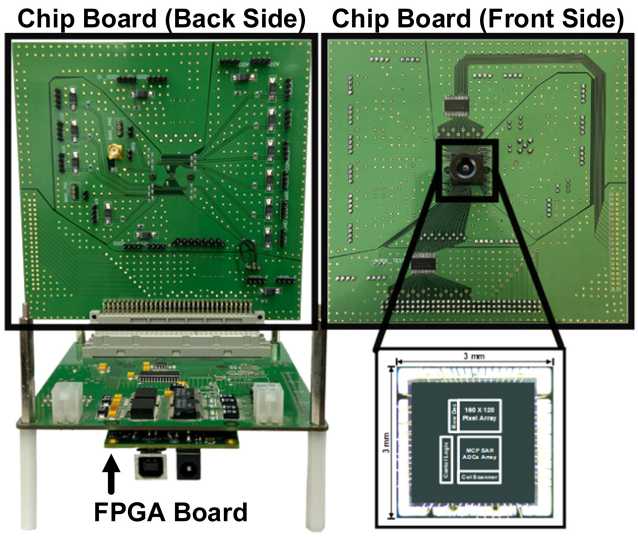

Fig. 8. Photograph of the measurement environment with the micro-photograph of the prototype chip.

period. The analog MUXs are controlled by $Ø_{CSEL}$, and it changes the readout direction depending on the even row ($Ø_{CSEL\_E}$) and odd row ($Ø_{CSEL\_O}$).

3. MEASUREMENT RESULTS

Fig. 8 shows a photograph of the testing CIS board with a microphotograph of the prototype chip. The chip was fabricated using a 0.18-μm CMOS process. A 160 × 120 pixel array with 4.4 μm pitch was implemented with 10 MCP readout channels, in which one SAR ADC covers 16 columns of pixels. The testing CIS board comprises a chip board and a field-programmable gate array (FPGA) board. The fabricated CIS chip was bonded to the chip board. To verify the performance of the prototype CIS, various types of control signals were generated by an external FPGA and supplied to the chip board by the FPGA board. The output codes of the chip board were transmitted to the PC through the USB interface and processed using a software program to display the real-time imaging on the screen. The capturing software program with various verification functions was customized using MATLAB programming.

Fig. 9. Captured sample image from the prototype CIS.

A sample image captured by the prototype CIS is shown in Fig. 9. The prototype CIS demonstrated a frame rate of 120 frame per second (fps) with a total power consumption of 1.92 mW. In the dark illumination condition, as in [14], 100 frames were captured to obtain the standard deviation of noise, resulting in 0.47 LSB_{rms}, corresponding to 413.1 μV_{rms}. The 10-bit SAR ADC has the full input range of approximately 0.9 V with 1-LSB of 880 μV. A fixed-pattern noise from the MCP readout pattern was removed using off-chip digital calibration [8,9]. The pixel rate of the prototype CIS is approximately 2.3 mega pixel per second (Mp/s). With the proposed biasing control method, compared to the conventional MCP readout, a power saving effect of 10.6% was confirmed in this study. The measured performance of the prototype CIS is summarized in Table 1.

The figure of merit (FoM) in terms of power efficiency and noise performance [15,16] is calculated as

$$FoM = \frac{Noise \times Power\ consumption}{Number\ of\ pixels \times frame\ rate} \quad (2)$$

From this, the developed CIS obtained an FoM of 344.3 μV·nJ. Table 2 shows the performance comparison with other works based on the 3T-APS pixel array. In terms of noise performances, it was confirmed that coupling noises between neighboring columns occurred owing to insufficient shielding. With further addition of the layout shielding pattern, the random noise will be reduced, resulting in further improved FoM. The measured performance of the prototype CIS is summarized in Table 1.

One of the layout issues in this work is that the input of the test ADC is laid without considering shielding across the global digital

Table 1. Performance summary.

Parameter	Value
Technology	0.18 μm CMOS Process
Chip area	3 × 3 mm
Supply voltages	3V (Pixel), 2.8V(Analog), 1.8V(Digital)
Power consumption	1.92 mW
Number of pixels	160 (H) × 120(V)
Pixel size	4.4 μm × 4.4 μm
Random noise	0.47 LSB_{rms}
ADC resolution	10 bits
ADC input range	0.9 V
Dynamic range	57.4 dB
Sampling rate	981 kS/s (post-simulation)
Frame rate	120
FoM	344.3 (μV·nJ)

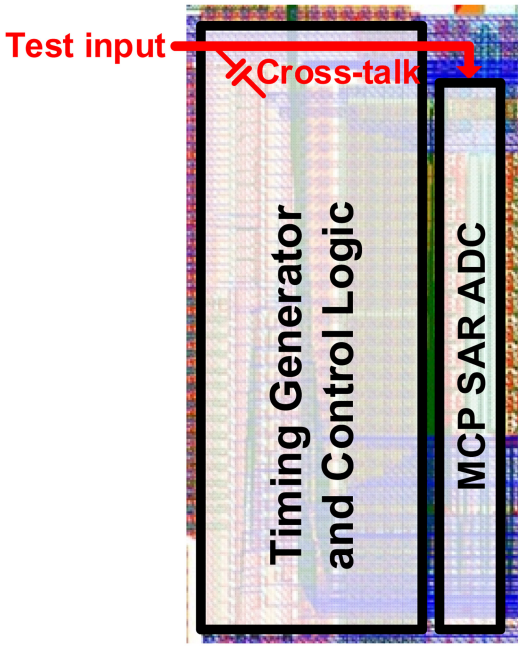

Fig. 10. Cross-talk issue with digital logic and test input.

logic and timing generator, as shown in Fig. 10. Therefore, it is difficult to evaluate the performance of the designed ADC alone, such as differential non-linearity (DNL), integral non-linearity (INL), and readout noise. This problem is expected to be solved sufficiently by modifying the layout pattern.

4. CONCLUSIONS

In this study, we proposed a delta readout SAR ADC optimized in the MCP readout structure. By alternating the MCP readout direction between the even and odd rows, additional memory for the row-to-row delta readout was not required, resulting in a reduced area of occupation. In addition, by applying different bias currents of a pre-amplifier according to the operating period, the power efficiency was improved compared to the previous work. This work is meaningful in that it overcomes the shortcomings of previous studies.

Table 2. Comparison of performances.

Parameter	[17]	[18]	This Work
Technology	180n CMOS	65n CMOS	180n CMOS
Number of Pixels	1280 × 800	920 × 256	160 × 120
Resolution (bits)	11	9	10
Random noise (μV_{rms})	1500	5300	413
Power consumption (mW)	40	1.1	1.92
FoM (μV·nJ)	1674	28147	344.3

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