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Development of Semiconductor Packaging Technology using Dicing Die Attach Film

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Abstract

Advanced packaging demands are driven by the need for dense integration systems. Consequently, stacked packaging technology has been proposed instead of reducing the ultra-fine patterns to secure economic feasibility. This study proposed an effective packaging process technology for semiconductor devices using a 9-inch dicing die attach film (DDAF), wherein the die attach and dicing films were combined. The process involved three steps: tape lamination, dicing, and bonding. Following the grinding of a silicon wafer, the tape lamination process was conducted, and the DDAF was arranged. Subsequently, a silicon wafer attached to the DDAF was separated into dies employing a blade dicing process with a two-step cut. Thereafter, one separated die was bonded with the other die as a substrate at 130 °C for 2 s under a pressure of 2 kgf and the chip was hardened at 120 °C for 30 min under a pressure of 10 kPa to remove air bubbles within the DAF. Finally, a curing process was conducted at 175 °C for 2 h at atmospheric pressure. Upon completing the manufacturing processes, external inspections, cross-sectional analyses, and thermal stability evaluations were conducted to confirm the optimality of the proposed technology for application of the DDAF. In particular, the shear strength test was evaluated to obtain an average of 9,905 Pa from 17 samples. Consequently, a 3D integration packaging process using DDAF is expected to be utilized as an advanced packaging technology with high reliability.

Keywords: Dicing die attach film, Packaging process, Tape lamination, Dicing, Die

1. INTRODUCTION

The increasing demand for reduction in semiconductor size has resulted in the continuous development of new packaging technologies [1]. With increased focus in reduction of die thickness (less than 100 μm) and package miniaturization, stacked die packaging technology has gained importance [2]. Conventional pastes are not suitable for stacked die packages in case of ultra-thin die because they result in paste bleeding, creeping effect at the edge of the chip, and contamination of the bonding pad [3]. Consequently, die attach films (DAFs) have been introduced as an alternative to tackle these problems. Moreover, the advantages of mounting a DAF at the wafer level are well known [4]. Accordingly, research to determine an optimized process for manufacturing a stacked die using a DAF has been steadily progressing [4-6]. Previous studies have found that sidewall chipping (during the dicing process) [4], two-step dicing methods [7-8], and curing temperature [5] were major factors affecting the reliability of stacked packaging. Thus, an optimal process technology suitable for DAF properties must be obtained. Therefore, this study was aimed to propose an optimal die stacking package process technology suitable for DAF properties.

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2. EXPERIMENTAL

2.1 Wafer and DDAF Preparation

Silicon wafers measuring 200 mm and 725 μm in diameter and thickness were used. As the experiments were focused on the packaging process technology using dicing die attach films (DDAFs), wafer characteristics such as orientation, type, resistivity, and patterned nature were ignored. The silicon wafers were ground to 100 μm using the silicon wafer backside grind process as this was the minimum thickness that could be handled and thus manufactured appropriately. DISCO's DGP8760 equipment was used for the grinding process, wherein a DDAF was produced through the combination of dicing and die attach films. Fig. 1 (a) shows a DDAF with a 9-inch circular die attach film merged into a dicing film in a roll, and the simplified

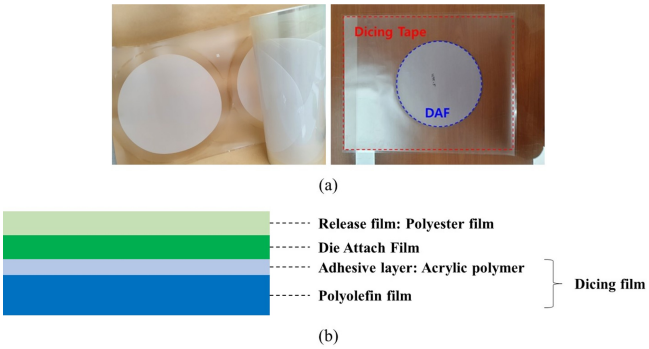

Fig. 1. (a) Image of the manufactured DDAF including a 9-inch circular DAF merged into a dicing film 30 cm × 30 cm and (b) schematic of basic structure of DDAF.

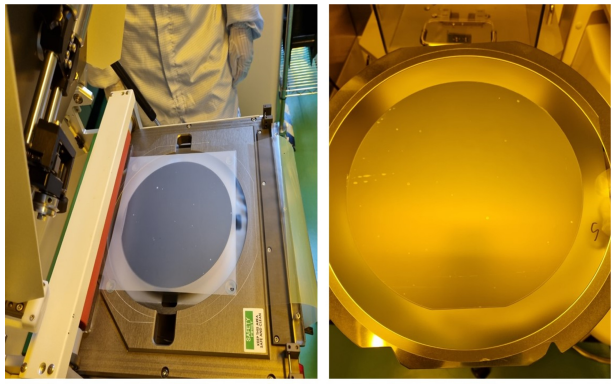

Fig. 2. (a) DDAF laminating process and (b) laminated wafer with the DDAF.

structure of the DDAF is shown in Fig. 1(b). The DDAF comprised dicing and die attach films with a total thickness of approximately 130 μm. Further, the dicing film was approximately 110 μm thick and comprised a polyolefin film and an acrylic polymer acting as an adhesive layer. In contrast, the thickness of the DAF was approximately 20 μm.

2.2 Tape Laminate Process

The DDAF was attached to a ground silicon wafer by employing a tape laminate process. The DYNATECH 8-inch manual wafer mount system was used for tape lamination. Following the installation of the manufactured DDAF roll on the equipment, the temperature of the chuck was set to 80 °C to satisfy the DDAF specifications. When the temperature of the chuck reached 80 °C, the ground wafer was placed on the chuck. However, there must be no pores on the wafers when attaching the DDAF; thus. wafers were cleaned of particles and dust beforehand. Subsequently, the DDAF was aligned with the wafer with the tape stretched to a sufficient degree before performing the laminating process. Fig. 2 shows the DDAF lamination process and laminated wafer with the DDAF.

2.3 Dicing Process

The dicing process was conducted to separate the DDAF-laminated wafer into dies based on the blade dicing method conducted using Disco Corp's DAD3350. The dicing process was performed as a two-step cutting method using two types of blades [7-8]. The thickness of the blade wheel, is referred to as kerf. This study used two types of blade kerfs: KH4-1435 (35 μm in length), and KH4-1435 (25 μm in length); both are manufactured by

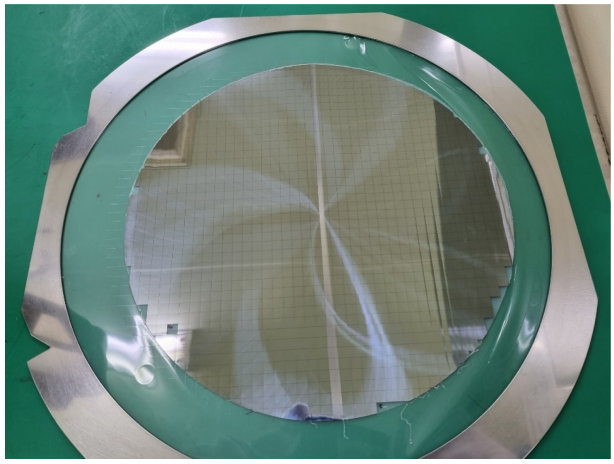

Fig. 3. The wafer with the DDAF attached. The wafer size is 8 inches, and the ring frame is 12 inches.

Kodis. In the two-step cut method, first, rough dicing was performed using the 35 μm blade kerf, followed by fine dicing using the 25 μm blade kerf. Further, the DDAF-laminated wafer was cut into half along its depth using the 35 μm blade kerf, and the 25 μm blade kerf was used to cut the remaining thickness of the wafer including the DDAF and a certain depth of the dicing tape. The dicing process was performed at 35,000 rpm and a feed speed of 50 mm/s. In addition, the two-step cut depth differed depending on the thickness of the wafers. Subsequently, the die size was divided into 5 × 5 and 10 × 10 mm^2.

2.4 Die Bonding Process

The bonding process employed a die-to-die bonding method (FC150, SET). As shown in Fig. 4, the die placed on the chuck was a 5 × 5 mm^2 and 10 × 10 mm^2, 100-μm-thick die with the

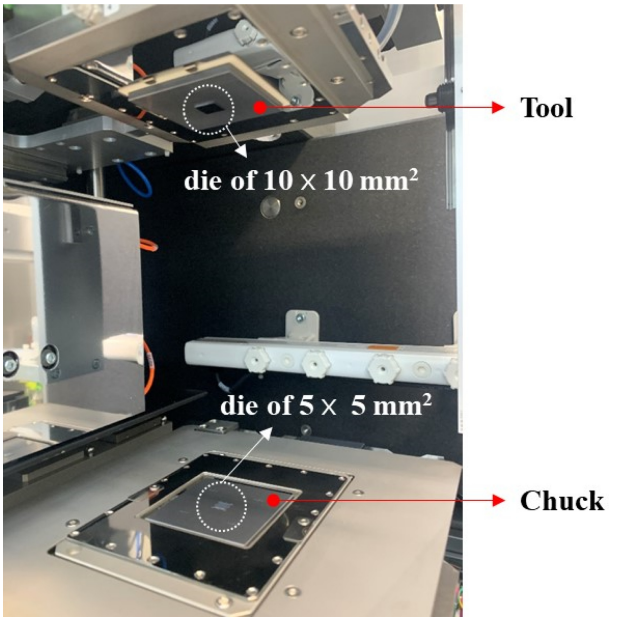

Fig. 4. Picture of die laminated with DAF mounted on chuck and die loaded on tool.

DAF laminated side facing up. The other die was a 10 × 10 mm^2, 725-μm-thick die turned over by a flipper and loaded into the tool (specimens created arbitrarily for die-stacked bonding). The bonding conditions were the application of a temperature of 130 °C for 2 s at a pressure of 2 kgf. Following bonding, the dies were placed in a vacuum oven (VAC-101P, Espec) at 120 °C for 30 min at a pressure of 10 kPa to remove air bubbles inside the DAF. Finally, the curing process was conducted at 175 °C for 2 h at atmospheric pressure using the same oven. The thermal curing process is necessary because delamination of the DAF owing to thermal expansion may result in mismatch of values of the interface [5, 9].

Thus, all processes were finished to complete two bonded chips. One substrate had a silicon size of 10 × 10 mm^2, 725-μm-thick, with the upper silicon chip measuring 10 × 10 mm^2, 100-μm-thick bonded with DAF (Fig. 5). The other substrate had a silicon size of 10 × 10 mm^2, 725-μm-thick, with the upper silicon chip measuring 5 × 5 mm^2, 100-μm-thick bonded with DAF (Fig. 6).

3. RESULTS AND DISCUSSIONS

Following the completion of all the processes, the appearance of the chips bonded by the DAF was observed using an optical microscope and FE-SEM. As shown in Fig. 5, no apparent abnormalities in appearance were observed. Fig. 6 shows the

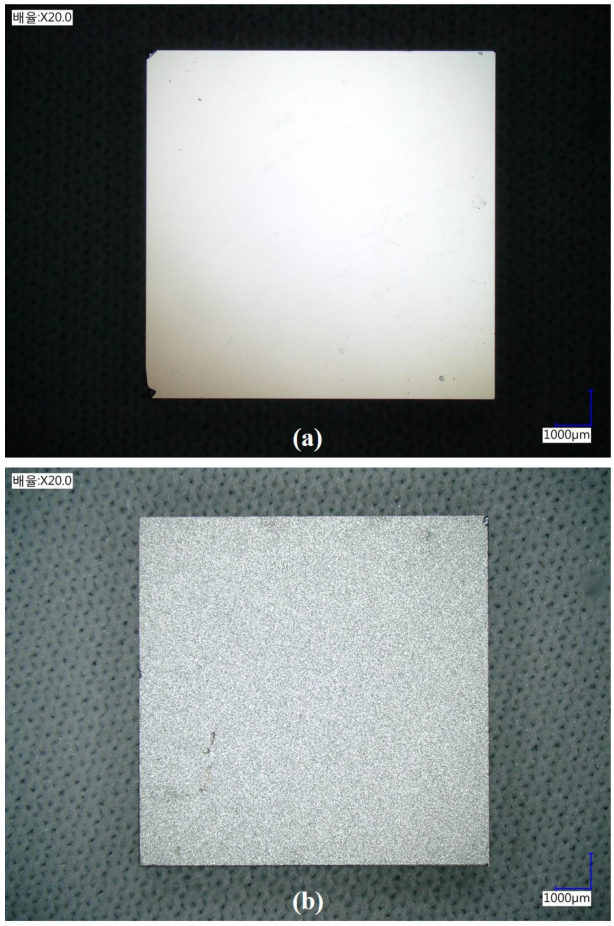

Fig. 5. (a) Optic image of the bonded chip's frontside and (b) Optic image of the bonded chip's backside.

observation with FE-SEM. The thicknesses of the lower substrate, DDAF, and upper chip were confirmed to be 725, 20, and 100 μm, respectively (Fig. 6 (a), (b)). Moreover, it is evident that the blade dicing process was performed in two steps at the enlarged die part. Further, a half-cut boundary was observed near 50 μm of the die thickness (Fig. 6 (c)).

Three experiments were conducted with the chips bonded by the DAF: 1) thermal stability evaluation, 2) constant temperature and humidity evaluation, and 3) shear strength test. First, the thermal stability evaluation was performed by placing the chip with a 100-μm-thick, 10 × 10 mm^2 die in an oven at 180° C for 24 h. Subsequently, the adhesion state of the DAF according to heat exposure was analyzed using scanning acoustic microscopy (SAM; Gen6, Sonoscan). Consequently, the constant temperature and humidity evaluation was performed by placing the chip with a 100-μm-thick, 10 × 10 mm^2 die in a chamber maintained at 85 °C and 85% relative humidity for 168 h (TH-TG-180, Jeiotech). Following the completion of the bonding process, decompression

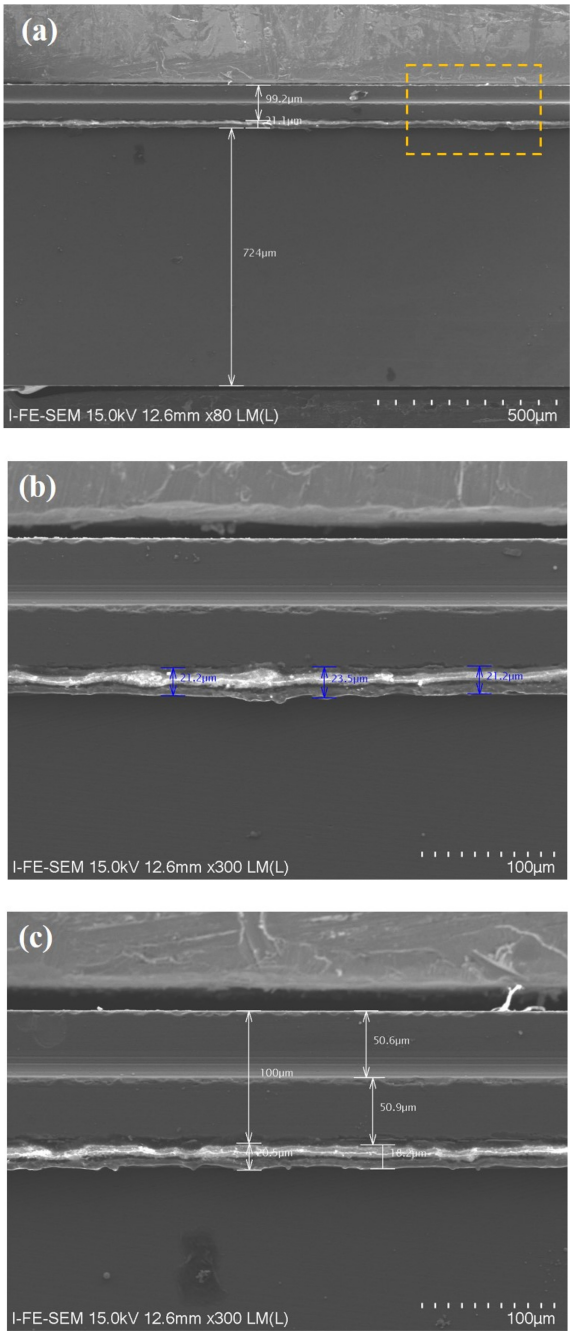

Fig. 6. (a) Bonded chip with substrate and die using DAF; (b) SEM image of DAF thickness; (c) half-cut boundary with two-step dicing process.

for defoaming, and final thermal curing process, SAM analysis was performed to confirm the DAF state after conducting the evaluations for thermal stability and constant temperature and humidity. As shown in Fig. 7, all DAF states in the three conditions were confirmed to be intact without adhesive voids. The SAM analysis was performed at a frequency of 150 MHz and a pixel size of 5 μm.

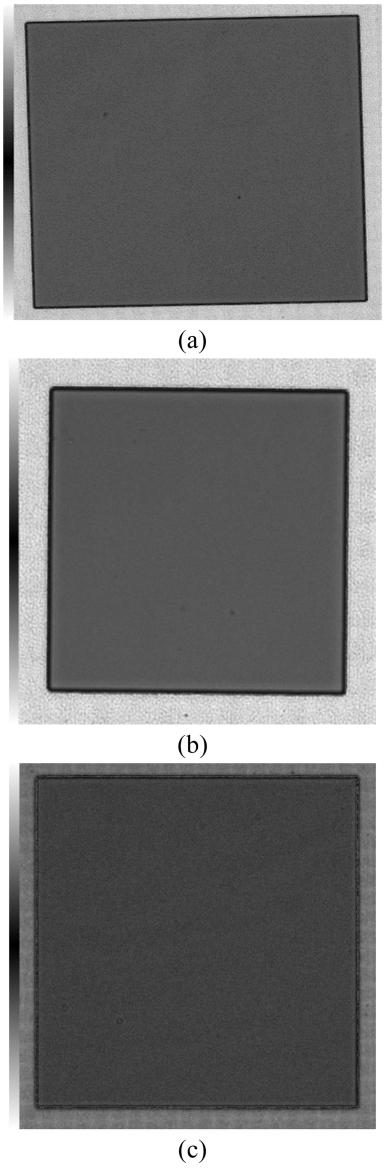

Fig. 7. SAM image of DAF state (a) for stacked chips, (b) after the thermal stability evaluation, (c) after the constant temperature and humidity evaluation. All chips are 10 × 10 mm^2 in size.

Next, the shear strength test (4000Plus, Nordson dage) was conducted to evaluate the durability during the application of a shear stress. The bonding chip mounted on the chuck was pushed out from the bonding surface between the 725-μm-thick, 10 × 10 mm^2 and 100-μm-thick, 5 × 5 mm^2 dies at a height and speed of 5 μm and 50 μm/s, respectively, using a tool. Subsequently, shear strength was obtained using the following formula.

$$\tau = F / A$$

where τ is the shear stress (kPa), F is the applied force (N), and A is the joint surface area (m^2).

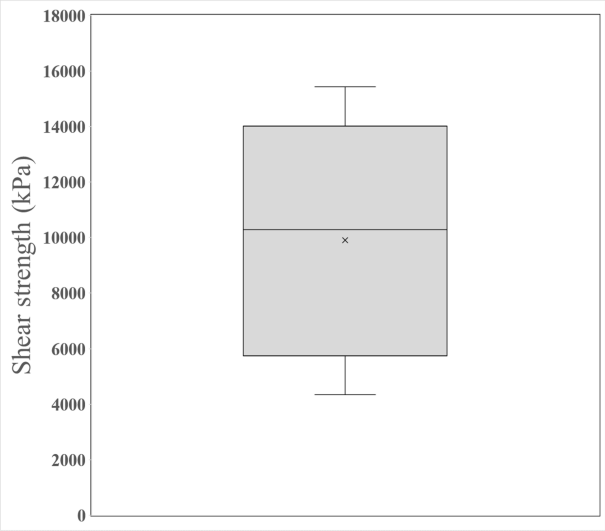

Fig. 8. Results of shear strength test.

The shear strength test evaluated 17 samples to obtain an average of 9,905 Pa, with maximum and minimum values of 15,430 and 4,340 Pa, respectively.

4. CONCLUSIONS

This study proposed a manufacturing process for die-to-die-bonded dummy chips using DDAFs. The analysis of the appearance of the manufactured die revealed no major problems in the appearance and cross-section of the bonded chips. In addition, the results of the analysis following thermal stability evaluation and constant temperature and humidity evaluation confirmed the absence of adhesive voids in the DAF state. Thus, an optimal process for the application of the DDAF was established, and it is expected to be utilized as an efficient semiconductor chip stacking technology.

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