

# A Self-Calibration Method for Time-Interleaved ADCs in High-Resolution LiDAR Systems without a Pilot Tone

Junseop Lee<sup>1</sup> , Sang-gyun Gi<sup>1</sup> , Yong Hwi Kim<sup>1</sup> , Seungjoo Lee<sup>1</sup>, and Jihyuk Cho<sup>1,+</sup> 

<sup>1</sup>IT Convergence System Research Center, Korea Electronics Technology Institute (KETI), 25, Saenari-ro, Bundang-gu, Seongnam-si, Gyeonggi-do, 13509, Republic of Korea

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**ABSTRACT:** High-resolution LiDAR systems need to acquire data at high speed to detect targets accurately and reliably, which can be achieved by using time-interleaved analog to digital converters (ADCs) (TI-ADCs). However, TI-ADCs constructed from independent sub-ADC chips suffer from a critical issues with ambiguity in the ordering of samples, which is caused by random inter-channel delays that arise from asynchronous initialization. In this study, we propose a self-calibration method without a pilot tone to resolve this ambiguity. The proposed method utilizes the capability of ADC devices to generate an internal test pattern in conjunction with a statistical analysis of repeated execution of serial programming interface (SPI) commands to measure and compensate for random startup delays to obviate the need for auxiliary analog hardware. The proposed method was validated through experiments using a custom dual HMCAD1511 ADC module with a sampling rate of 2 GSps. The experimental results show that the proposed method was able to correct the sample sequence reliably across various input waveforms and maintain stability over long-term operation under varying ambient temperatures. Furthermore, an average calibration time of 643 ms was achieved. The resulting calibrated ADC module provides a cost-effective and flexible solution for the development of high-performance, high-resolution LiDAR systems.

**KEYWORDS:** *High-speed time-interleaved ADC, High-resolution LiDAR system, Sample ordering, Digital calibration*

## 1. INTRODUCTION

LiDAR technology is a key perception sensor in applications such as autonomous driving, robotics, and high-precision 3D mapping systems [1,2]. These applications require LiDAR with high range resolution to detect objects efficiently [3]. Two prominent approaches have been developed to implement high-resolution LiDAR, including the full-waveform method, which digitizes the entire backscattered optical signal, and the frequency-modulated continuous-wave (FMCW) method. By providing rich information about the target, these techniques significantly improve detection accuracy and reliability. However, they also introduce the technical challenge of requiring analog-to-

digital converters (ADCs) with gigasample-per-second (GSps) sampling rates [4-6].

Time-interleaved ADC (TI-ADC) architectures have been introduced as a practical solution to achieve such high sampling rates by operating multiple sub-ADCs in parallel to increase the overall sampling rate [7]. The digital data interface between ADC and field-programmable gate array (FPGA) devices is a key consideration in integrating high-speed TI-ADCs. Most contemporary high-performance ADCs have adopted the JESD204B/C serial interface, which implements the JEDEC standard [8]. This standard supports multi-gigabit data rates and enables high-bandwidth communication with a low pin count. Moreover, the protocol includes built-in features for deterministic latency and lane synchronization, which ensures data alignment across multiple devices at the interface level [9,10].

However, the JESD204B interface involves several disadvantages of note. The interface requires high-performance transceiver I/O and a physical layer (PHY) within the FPGA, and its complex protocol stack consumes significant logic resources [11]. This resource consumption can constrain the logic available for the signal processing required to analyze

<sup>+</sup>Corresponding author: jcho@keti.re.kr

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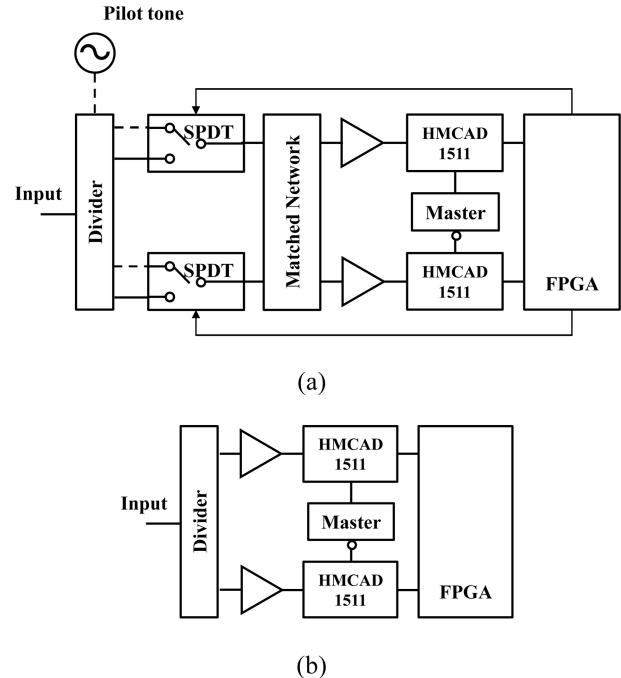
LiDAR data in practical implementations. Furthermore, reliable implementation often depends on proprietary intellectual property (IP) cores and drivers, which increases the costs and complexity of developing such systems [12].

As an alternative to that approach, the traditional parallel low-voltage differential signaling (LVDS) interface remains a viable option for many systems. LVDS transmits data directly at the physical layer without a complex protocol stack, which results in a simpler FPGA implementation, lower resource utilization, and no additional IP licensing costs [13]. This simplicity, however, means that the interface lacks an inherent protocol for data synchronization. Consequently, when a TI-ADC is implemented at the board level with separate sub-ADCs, the asynchronous power-up sequence and independent internal phase-locked loop (PLL) operation of each chip lead to ambiguity in the initial sample ordering that must be addressed at the system level [14].

The most conventional method to correct for channel mismatches in LVDS-based TI-ADCs is to inject a precision pilot tone into the system [15,16]. However, this approach requires additional analog circuits such as pilot-tone generators and multiplexers, which increases the cost and complexity the hardware. It also involves the inherent limitation of introducing an insertion loss into the signal path, which can degrade the overall signal-to-noise ratio (SNR) of the system [17].

Several blind background calibration techniques that exploit the statistical properties of the input signal itself to overcome these limitations have also been investigated [18,19]. These techniques primarily correct for sub-sample-level fine timing skew or gain/offset mismatches by either minimizing the correlation between adjacent channel outputs [18] or utilizing signal derivative statistics [19]. Although these techniques implicitly assume a correctly aligned sample order, they do not address the ambiguity in the initial sample ordering itself. Thus, the sample ordering must be corrected before conventional fine-mismatch calibration can be applied. This poses a critical challenge, especially for LiDAR applications that require precise temporal integrity.

In this study, we propose a self-calibration method for a TI-ADC module based on the HMCAD1511 converter manufactured by Analog Devices to resolve the inherent problem with sample ordering while retaining the low cost and implementation advantages of the LVDS interface. The proposed method operates entirely in the digital domain and does not require pilot tones or additional analog circuitry. This provides a practical and low-cost solution to reconstruct the correct data sequence from discrete ADCs reliably. Thus, this work establishes a foundation for the implementation of high-resolution LiDAR data acquisition systems.



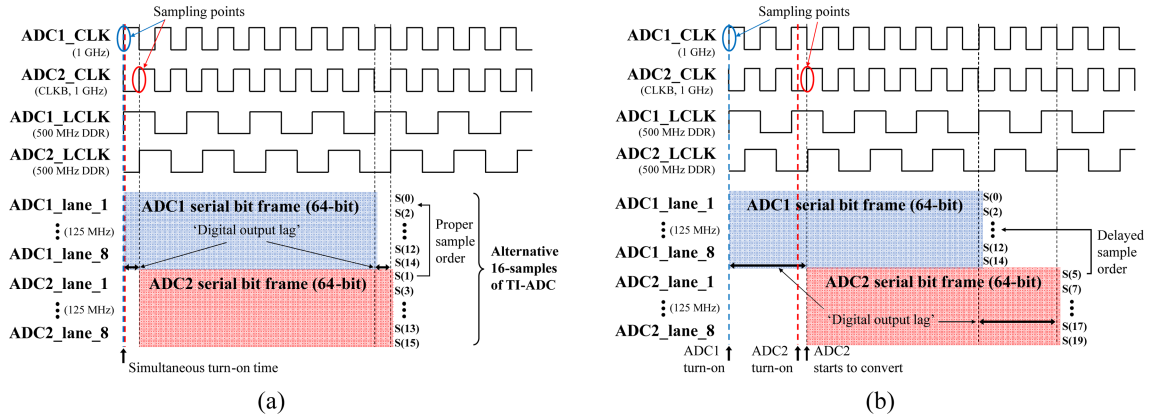
**Fig. 1.** HMCAD1511-based TI-ADC calibration hardware: comparison of hardware structures between (a) conventional and (b) proposed calibration methods.

## 2. PRINCIPLE OF CALIBRATION METHOD

### 2.1 Calibration without a Pilot Tone

Fig. 1 illustrates the difference between conventional calibration hardware and the proposed design for an HMCAD1511-based TI-ADC. The conventional method consists of power divider circuits for both the input signal and a pilot tone, two single pole, double throw (SPDT) switches to implement a high-speed multiplexer, a matching network to perform impedance matching with the ADC front end, and FPGA logic for control and data alignment (Fig. 1(a)). Because TI-ADCs sample the signal at high speed, the power divider and multiplexer circuits should also exhibit wideband characteristics. The implementation of circuits that exhibit wideband characteristics, low insertion loss, and high gain flatness typically requires expensive components. In a time-of-flight (ToF) LiDAR system based on time-domain signals, an attention of 1 dB can cause a signal loss of approximately 11%. Therefore, some reduction in SNR is inherently unavoidable in the conventional approach. The proposed structure eliminates this lossy analog circuitry and thus offers some notable advantages in terms of both cost and SNR.

Fig. 2 shows the timing relationship between the clock signals and the digital output data for each HMCAD1511 ADC. The analog sampling clocks (CLK and CLKB) are

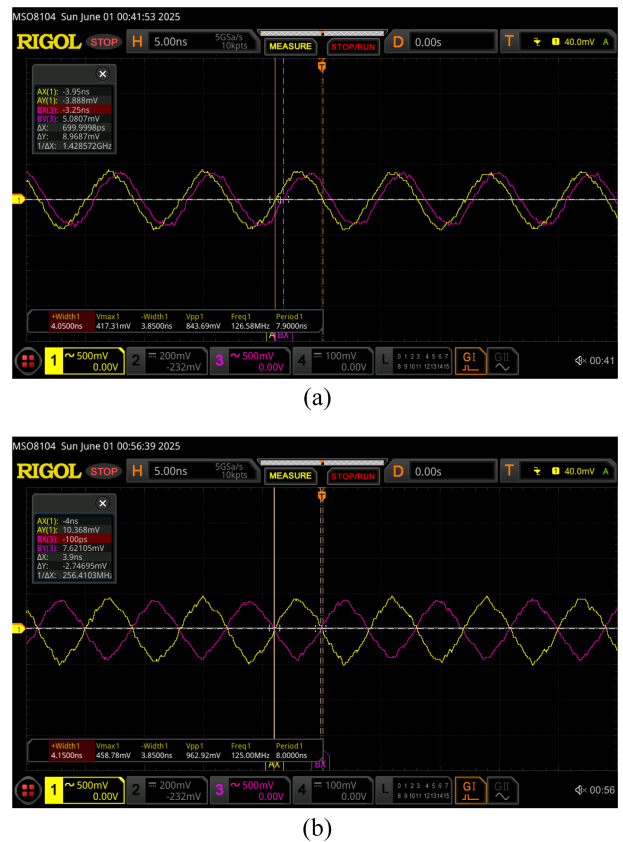


**Fig. 2.** A conceptual timing diagram of two HMCAD1511 ADCs: (a) no startup delay ambiguity and (b) a delay of 2 clock cycles in the first ADC.

supplied to the ADCs with mutually inverted phases. The digital clock for LVDS (LCLK) is generated internally by the ADC with a period twice that of CLK. The eight parallel LVDS lanes from each ADC sequentially generate the output comprising 8-bit samples. Consequently, a total of 64 bits of data from each ADC constitutes a single frame, which is transmitted over every eight CLK cycles, and the frame clock (FCLK) is synchronized to this period.

Although the input sampling clocks (CLK and CLKB) are supplied to each ADC with a fixed, inverted phase relationship, the digital clocks (LCLK and FCLK) are not synchronized between the devices due to the independent lock-up latency of each internal PLL. Given this lack of synchronization, digital initialization results in a nondeterministic ordering of output data regardless of the analog clock. For an ideal scenario without startup delay as shown in Fig. 2(a), a fixed digital output delay is present that corresponds to the inverted clock phase. Such deterministic delays can be readily calibrated in the FPGA logic using a synchronizer. However, when a random delay occurs as illustrated in Fig. 2(b), the delay must be measured with some method to perform a calibration. This is analogous to the function of a pilot tone in conventional calibration schemes. As shown in Fig. 3, the results of measuring a random delay in the frame clock confirmed this ambiguity, with delays of 0 and 3 ns being observed in different power cycles.

The proposed method digitally measures and compensates for the random delay in each boot-up sequence without using a pilot tone. Fig. 4 illustrates the relationship between the timing of the output data of each ADC and the constituent delay components. A frame delay is defined as a delay equivalent to an integer number of 8-bit data frames, whereas a fine delay is a sample-level, sub-frame delay caused by the lag of the digital clock. The total delay can be expressed as the sum of a fixed 0.5-ns delay caused by the inverted input clocks



**Fig. 3.** The result of frame clock delay measurement: startup delay ambiguities in frame clock of (a) 0 ns and (b) 3 ns, respectively.

(CLK and CLKB) and the measured frame and fine delays.

The fine delay is determined by counting the phase difference between the FCLK signals of the two ADCs. In contrast, the frame delay can be measured using the test pattern feature provided for timing skew correction, which is a function common to ADCs with LVDS interfaces. As shown in Fig. 5, the frame delay of the HMCAD1511 that affects the

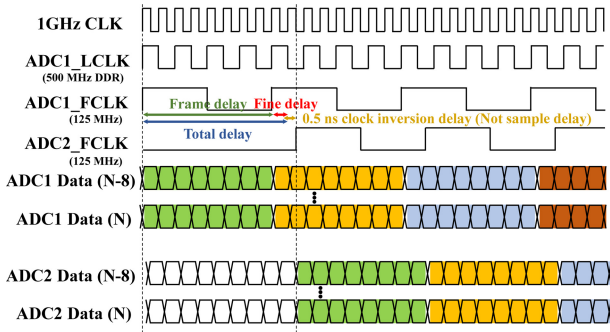


Fig. 4. Illustration of delay components between two ADCs.

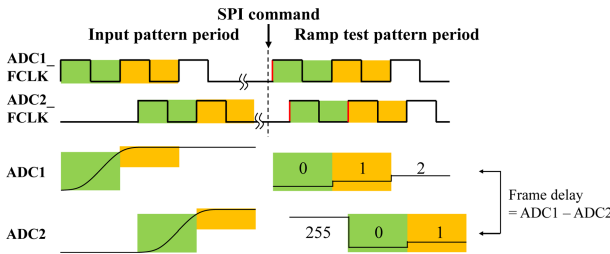


Fig. 5. Correlation between input and test pattern delays.

input signal is also equivalently present in the test pattern. A ramp test pattern is generated simultaneously from each ADC, which outputs a constant value for one frame. Consequently, the frame delay can be determined from the difference between the two output values for any given pattern frame.

The test pattern is typically generated by setting ADC registers via an SPI command. The transmission timing of the command relative to the internal operation of the ADC determines the delay between the patterns. Assuming the SPI clock from the FPGA is asynchronous to the LVDS digital clock of the ADCs, the SPI command can be issued at three distinct moments relative to the operational timing of the two devices, as illustrated in Fig. 6. These moments are categorized as Case I and Case III when the command precedes or succeeds the operational window of both ADCs, respectively, and Case II when it is issued between them. In Cases I and III, the ADCs generate their test patterns in immediate succession after the command. In Case II, however, the test pattern from the trailing ADC is generated one frame later. These characteristics are exploited by repeatedly issuing the SPI command and compiling the relative frequency of the measured frame delays for Cases I, II, and III to determine a statistical histogram. The resulting distribution corresponds to the ratio of the fine delay to the frame clock period, which allows for the determination of the true frame delay to resolve the ambiguity. It should be noted that this method is not applicable if the SPI clock is correlated with the ADC's digital clock. A specific case being triggered consistently prevents the

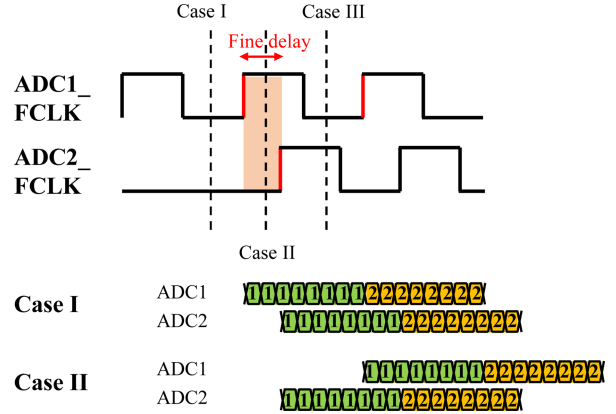


Fig. 6. The output of each ADCs depending on three different cases of SPI command timing.

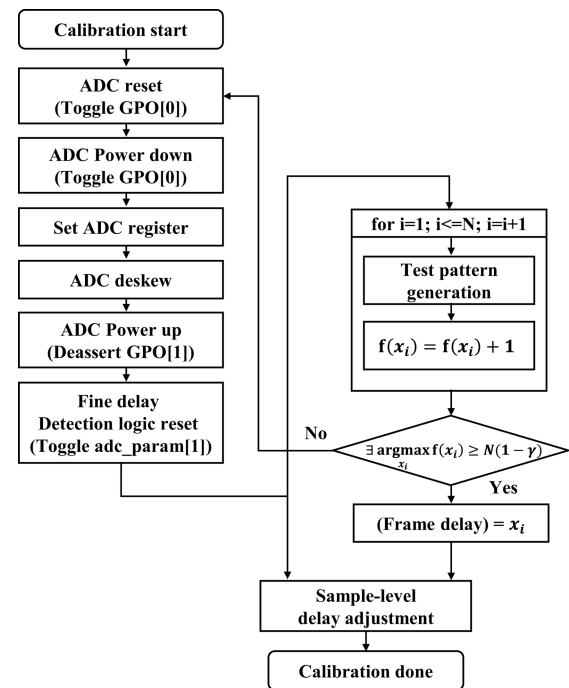


Fig. 7. Flowchart of TI-ADC delay calibration.

formation of a statistical distribution and leads to an indeterminate measurement. However, a low-speed SPI clock asynchronous to the digital clock of the ADC can be easily generated within the same device given that the LVDS interface for a high-speed ADC typically requires a logic device for signal conditioning.

The algorithm used to determine the total delay is illustrated in the flowchart shown in Fig. 7. The calibration sequence is initiated by configuring the ADCs, after which the logic for measuring the fine delay is activated. Subsequently, the frame delay measurement logic is enabled, and the validity of the measured frame delay is evaluated. The algorithm either iterates by re-initializing the ADCs or concludes the calibration

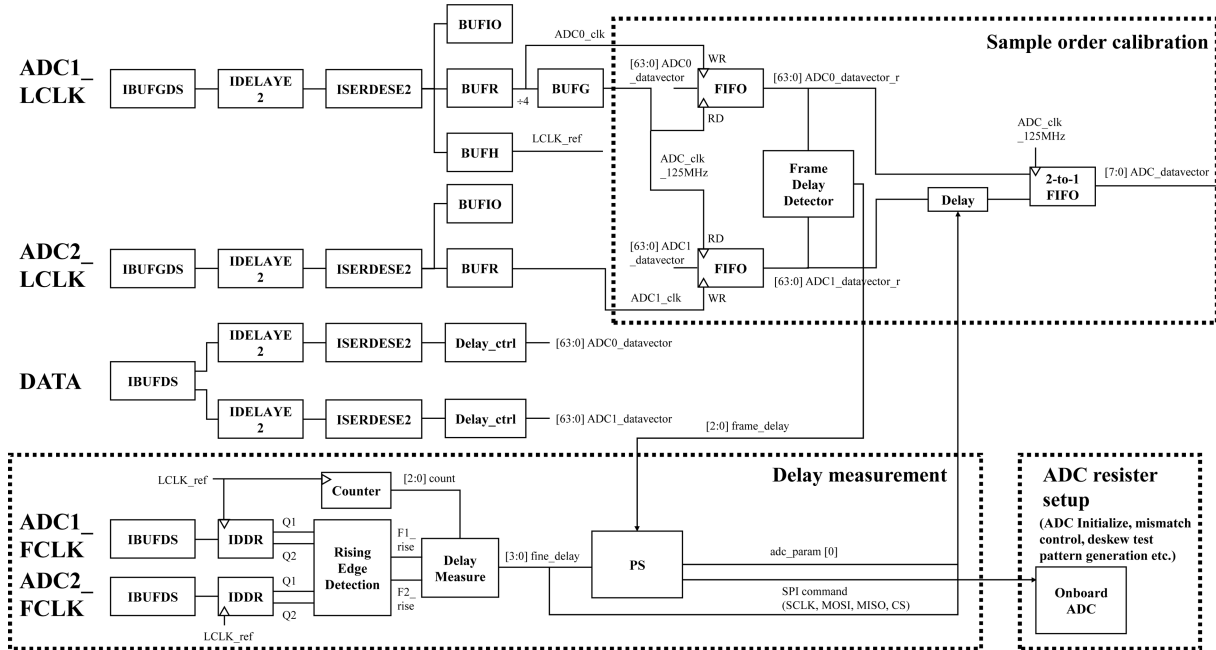


Fig. 8. Overall structure of FPGA delay calibration logic.

depending on the results of the validation.

The fine delay ratio  $\gamma$  to determine the statistics for the cases of SPI command timing is given by

$$\gamma = \frac{\tau_{\text{fine}}}{\tau_{\text{FCLK}}}, \tag{1}$$

where  $\gamma$  is the fine delay ratio,  $\tau_{\text{fine}}$  is the fine delay, and  $\tau_{\text{FCLK}}$  is the period of frame clock. For example, with the output of HMCAD1511 ADCs, 8 nanoseconds of  $\tau_{\text{FCLK}}$  and 2 nanoseconds of  $\tau_{\text{fine}}$  yields a  $\gamma$  of 0.25.

As the desired frame delay corresponds only to Cases I and III, the discriminant for determining the proper criterion for the valid frame delay is developed as follows.

$$\frac{\text{argmax}_i f(x_i)}{N} \geq 1 - \gamma \tag{2}$$

where  $N$  is the number of maximum iterations during the frame delay search,  $x_i$  is the  $i^{\text{th}}$  histogram bin of the frame delay measurements, and  $f(x_i)$  is the frequency of a corresponding bin  $x_i$ .

### 2.2 Hardware Implementation

An integrated hardware module for a high-resolution LiDAR system was developed to implement and validate the proposed self-calibration method using an Analog Devices HMCAD1511 chip and an AMD Zynq-7030 FPGA, as shown in Fig. 9. A sampling clock of 1 GHz for each ADC was supplied with mutually inverted phases.

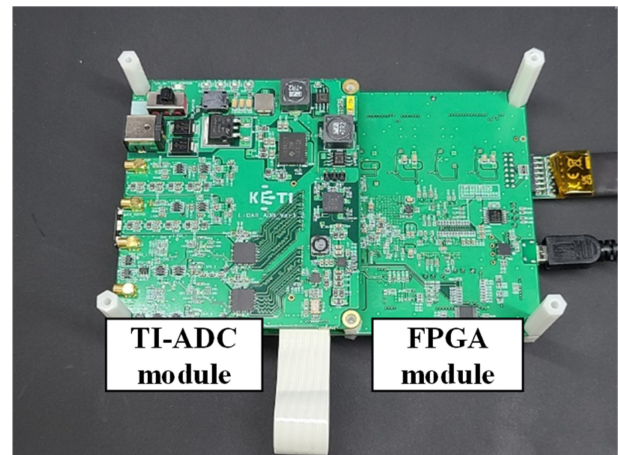
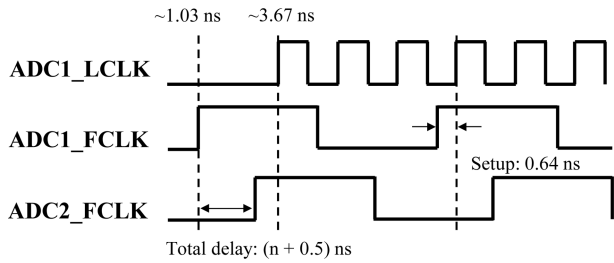


Fig. 9. Implementation of TI-ADC module with an FPGA processor.

Fig. 8 depicts the overall architecture of the delay calibration logic implemented in the FPGA, which comprises two main parts, including a delay measurement block and a sample-order calibration block. The Zynq™ processing system (PS) is used to assist with ADC control and delay calculations. For each data lane, the timing skew of the LVDS interface is corrected using buffers and tapped-delay elements, and a serial-to-deserializer is used to parallelize the acquired ADC data. To serve as a low-skew reference clock for delay measurement, LCLK is routed using the BUFR and BUFG primitives to minimize its propagation delay. The measured delay parameters are then fed into a calibration logic block for dynamic data realignment.



**Fig. 10.** Setup time condition for the input delay path of fine-delay measurement logic from static timing analysis.

**Table 1.** Resource utilization on the Zynq-7030 FPGA for the proposed calibration method

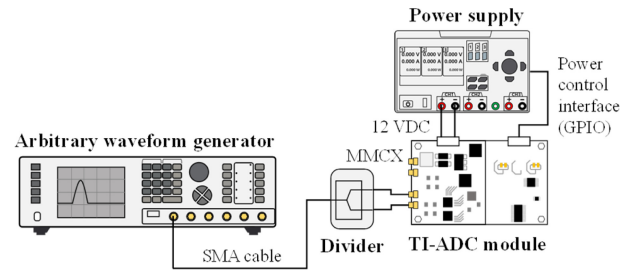
Resource	Utilization (Units)	Available (Units)	Utilization (%)
LUT	1,571	78,600	1.9
FF	1,189	157,200	0.7
BRAM	4	265	1.5
BUFG	3	32	9.3
IO	4	163	2.4

Due to the maximum operating frequency constraints of the Zynq-7030 chip, the fine delay measurement logic was constructed using an IDDR primitive to sample the frame clock with the 500 MHz LCLK to achieve an equivalent sampling rate of 1 GHz. An edge detection logic subsequently doubles the resolution of a 500 MHz counter to create the equivalent of a 1-ns timer, which measures the interval between the rising edge of the first ADC's FCLK and that of the second. The setup time margin for this counter logic is shown in Fig. 10. The delay of the LCLK through the BUFH was approximately 3.67 ns, and the delay of the FCLK through the IBUFDS was approximately 1.03 ns. This provides a setup time of approximately 0.64 ns, which ensures that the variable total delay can be sampled safely without metastability. The hold time condition was not considered in this logic because the FCLK pulse width is significantly longer than the LCLK period, and only the rising edge is detected. Table 1 summarizes the total resources used in the design implemented with Zynq-7030 devices.

### 3. RESULTS AND DISCUSSION

#### 3.1 Hardware-in-the-loop Measurement Setup

The TI-ADC hardware module implemented with the proposed method was verified using the hardware-in-the-loop (HIL) measurement environment shown in Fig. 11. An Agilent 81180A arbitrary waveform generator (AWG) was used to generate simulated LiDAR signals and other test waveforms.



**Fig. 11.** Hardware-in-the-loop measurement environment setup for the verification of calibration method.

The output of the AWG was evenly split by a Mini-Circuits ZX10-2-42-S+ power divider and supplied to the input of each ADC. A RIGOL DP932A power supply provided 12 V DC to the TI-ADC module. A Linux-based control program was implemented on the processing system of the Zynq-7030 FPGA to automate the measurements by controlling the power supply and logging the status information to an SD card.

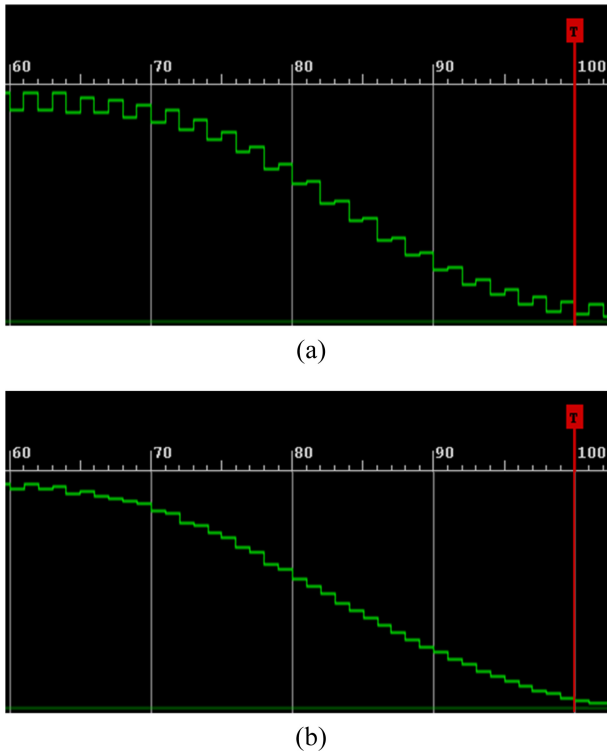
#### 3.2 Sampling Results under Various Types of Waveforms

The operation of the proposed calibration method was verified by comparing the data acquired before and after calibration using a monotonically varying rapid pulse edge signal. As shown in Fig. 12, for the falling edge of a pulse, the data stream from the second ADC preceded that of the first by one sample before calibration, resulting in a non-monotonic sequence. After calibration, however, a monotonically decreasing sequence was observed, which confirms that the sample order between the two ADCs was correctly aligned.

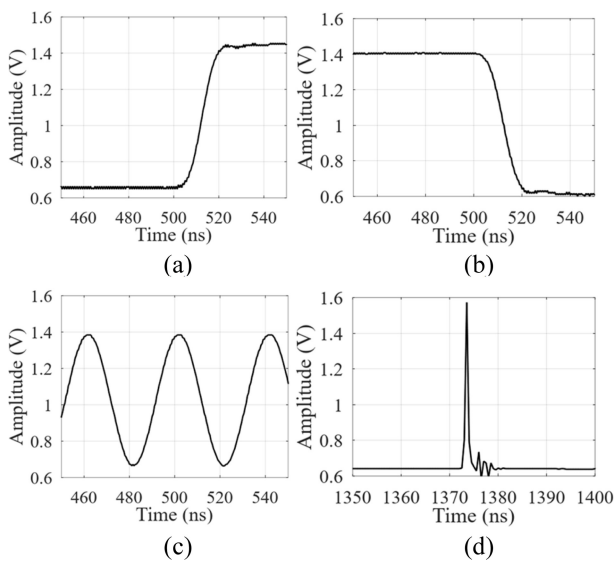
The same measurement techniques were performed repeatedly for a variety of waveforms to validate the calibration method for other types of signals. The results are illustrated in Fig. 13. The signal sources included rising and falling pulse edges, a 25-MHz sinusoidal waveform, and a short pulse with a full width at half maximum (FWHM) of 820 ps to simulate a LiDAR echo. The sample order was correctly calibrated for all of the applied waveforms. The explicit result of the impulse-like LiDAR echo signal sampled by the implemented 2-GSPS TI-ADC, shown in Fig. 13(d), particularly reinforces the requirement for high-speed data acquisition in high-resolution LiDAR systems.

#### 3.3 Long-term Stability Verification

The long-term operational stability of the proposed calibration method needed to be verified because it is based on a statistical technique. Thus, we conducted an experiment to

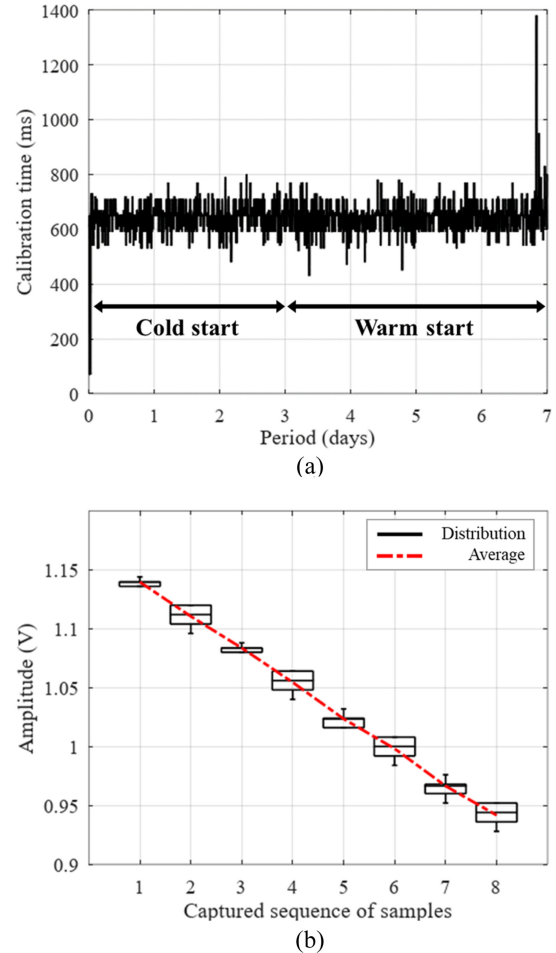


**Fig. 12.** The sequence of samples captured in Vivado™ hardware manager: monotonically decreasing pulse edge samples (a) before and (b) after the calibration process.



**Fig. 13.** Measured data from calibrated TI-ADC on various type of waveforms: (a) rising edge of a pulse, (b) falling edge of a pulse, (c) 25 MHz sinusoidal waveform and (d) 820 ps (FWHM) short pulse.

evaluate the long-term effects of our approach over a period of one week under varying thermal conditions. The ambient temperature was maintained at approximately 25°C during the day with an air conditioner (A/C) and allowed to rise to a



**Fig. 14.** Long-term stability test results over one week: (a) Calibration time and (b) the distribution of captured data.

maximum of 35°C at night without A/C. For the first three days, the measurement system was operated under cold-start conditions. The module was then turned on and off under warm-start conditions for the subsequent four days to allow the temperature of the chip to saturate at approximately 58°C post-boot. The falling edge of a pulse was used as the test waveform, with the system configured to record data around a 1.05-volt threshold corresponding to the pulse midpoint. The calibration timeout was set to 60 s, and a trial was logged as a failure if the time exceeded this limit or if the resulting sequence was determined to be non-monotonic.

The results of the week-long test are shown in Fig. 14(a). The calibration time ranged from a minimum of 70 ms to a maximum of 1.38 s, with an average of 643 ms. No timeout failures were recorded. The majority of the measurements clustered around the average value. The appearance of outliers was not correlated with the experimental conditions such as ambient temperature or start-up condition, which suggests these factors had no observable influence.

Fig. 14(b) shows the amplitude distribution of the pulse edge

samples measured near the threshold level. No failures resulting from non-monotonic sequences were recorded. The box plot shows distinct and non-overlapping sample sequences with a monotonic decrease, which provides evidence for the successful outcome.

## 4. CONCLUSIONS

In this study, we have proposed a robust and efficient digital self-calibration method and verified its effectiveness to resolve the ambiguity in the ordering of initial samples that occurs when implementing a TI-ADC with separate sub-ADC components. The proposed technique automatically measures and calibrates for random delays at each boot-up by utilizing the ADC's internal test pattern feature and the statistical properties of SPI communication timing, which obviates the need for costly pilot-tone generators or wideband analog switch circuits. The validity of the method was demonstrated through a hardware module built with dual HMCAD1511 ADCs and a Zynq-7030 FPGA for a practical 2-GSPS TI-ADC implementation. The experimental results confirmed that the sample order was successfully corrected for various waveforms, including pulses, sinusoidal waves, and simulated LiDAR echo signals. Furthermore, a stability test conducted over a period of one week demonstrated that the calibration was completed reliably within an average time of 643 ms regardless of temperature variations. This calibration time is well within the typical boot-up period of an embedded system and a single execution at each power-on sufficed to ensure a reliable data sequence. The proposed approach provides a purely digital, low-cost calibration method, which we expect to serve as a practical foundational technology for developing high-resolution LiDAR data acquisition systems to resolve issues with hardware complexity and signal loss. Furthermore, we anticipate that future multi-channel extensions for ultra-high speed applications can be implemented with a hierarchical calibration process through a “divide and conquer” approach based on a thorough analysis of the statistical complexity of SPI command timing.

### CRedit Authorship Contribution Statement

**Junseop Lee:** Conceptualization, Data curation, Formal analysis, Investigation, Methodology, Software, Validation, Visualization, Writing – original draft. **Sang-gyun Gi:** Conceptualization, Writing – review and editing. **Yong Hwi Kim:** Software. **Seungjoo Lee:** Funding acquisition, Project administration, Resources, Supervision. **Jihyuk Cho:** Conceptualization, Resources, Supervision, Writing – review and editing.

### Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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