REVIEW

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Virtual Fabrication for Semiconductor Sensor Development: Process Modeling and Design Optimization

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ABSTRACT: The development of advanced semiconductor sensors faces increasing challenges due to process complexity, dimensional scaling, and difficulties in applying mature CMOS process design kits to specialized sensor applications. Virtual fabrication has emerged as a transformative approach for design-technology co-optimization (DTCO) in semiconductor sensor development. This comprehensive review examines virtual fabrication methodologies and their practical applications in process optimization, covering fundamental simulation approaches, process modeling techniques, and case studies across diverse sensor technologies. We analyze key process steps, including lithography with photoresist selection considerations, etching with quality-factor dependencies in MEMS sensors, deposition, chemical-mechanical polishing, and bonding. Case studies demonstrate the fabrication of aluminum nitride microcantilevers, wafer-level vacuum packaging, and hybrid bonding optimization. Virtual fabrication enables significant reductions in development costs, time, and experimental iterations while improving process yields from 30% to 90% in practical applications. Statistical and optimization methods complement physics-based simulations, providing efficient analysis of multi-parameter process spaces. Current challenges include the complexity of multi-scale modeling, computational costs, and the limited availability of non-standard process data. Future directions emphasize enhanced computational efficiency, real-time process monitoring integration, and comprehensive development of a process design kit for sensor applications.

KEYWORDS: *Virtual fabrication, Semiconductor process, MEMS Sensors, Process optimization, DTCO*

1. INTRODUCTION

The semiconductor industry continues to advance Moore's Law through aggressive scaling and innovative three-dimensional (3D) device architectures [1,2]. However, semiconductor sensor development presents unique challenges that distinguish it from conventional CMOS manufacturing. Unlike mature CMOS processes with well-established process design kits (PDKs), sensor fabrication often requires specialized processes, including deep reactive ion etching, anisotropic wet etching, wafer-level packaging, and heterogeneous integration [3]. These processes exhibit complex dependencies on design parameters, material properties, and process conditions that are difficult to predict through traditional trial-and-error approaches.

The escalating cost of semiconductor fabrication facilities, with modern fabs requiring capital investments exceeding billions of dollars, makes experimental process development increasingly prohibitive. A single mask set for advanced nodes can cost millions of dollars, and each process iteration requires weeks to months of fabrication time followed by extensive characterization. This traditional develop-fabricate-test cycle creates substantial barriers to innovation, particularly for specialized sensor applications where production volumes may not justify dedicated process development.

Virtual fabrication has emerged as a powerful paradigm shift that addresses these challenges by enabling comprehensive process modeling and optimization in silico before committing to physical fabrication [4,5]. Virtual fabrication platforms, such as SEMulator3D and Synopsys Process Explorer, provide the capability to transform two-dimensional layout designs into accurate 3D process simulations. These platforms incorporate physics-based

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models for fundamental semiconductor processes, including etching, deposition, lithography, and planarization, enabling the prediction of final device geometry, electrical characteristics, and potential failure modes.

Statistical analysis methods and machine learning techniques complement virtual fabrication by enabling the efficient exploration of multi-dimensional parameter spaces, the identification of process correlations, and the development of predictive models [6-20]. However, their role remains one of optimization and analysis tools built upon the foundation of physics-based simulations. Recent systematic reviews have documented the growing adoption of these computational approaches across semiconductor manufacturing, including applications in virtual metrology, process control, defect detection, and yield prediction.

Design-Technology Co-Optimization (DTCO) has become essential for advanced semiconductor development, enabling the simultaneous optimization of device design and manufacturing processes [21-28]. For sensor applications where standard CMOS PDKs are often inadequate, DTCO facilitated by virtual fabrication becomes crucial. Virtual platforms enable designers to explore the impact of process variations on sensor performance, identify critical process steps, and optimize designs for manufacturability before tape-out.

This comprehensive review examines the state of the art in virtual fabrication for semiconductor sensor process development. We begin by establishing the fundamental principles of virtual fabrication and key simulation methodologies. We then explore process-specific modeling approaches for critical fabrication steps, including etching, deposition, chemical mechanical polishing, and bonding. Statistical optimization methods, including the design of experiments and multi-objective optimization, are examined as complementary tools that enhance virtual fabrication capabilities. Practical applications are illustrated through case studies of aluminum nitride microcantilever sensors [29], wafer-level vacuum packaging for quantum sensors [30], and advanced hybrid bonding for 3D integration [31,32]. Finally, we discuss current limitations and future research directions to advance the field toward comprehensive virtual process development environments.

2. VIRTUAL FABRICATION FUNDAMENTALS

Virtual fabrication represents a computational approach to semiconductor process modeling that enables the prediction of device structures and characteristics without physical wafer processing [5]. The fundamental concept involves transforming design layouts through sequential process simulations that model the physical and chemical phenomena occurring during actual fabrication. This section examines the core principles, simulation methodologies, and commercial platforms that constitute modern virtual fabrication capabilities.

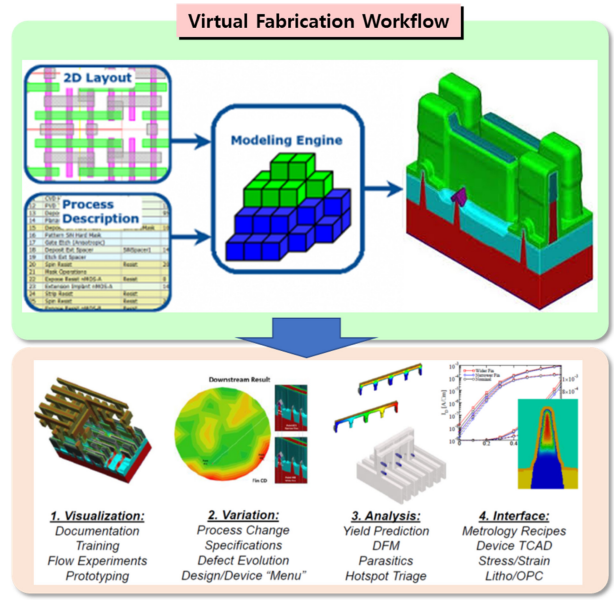

Fig. 1. Virtual fabrication workflow from 2D layout to 3D process simulation, Adapted from Ref. [42].

The virtual fabrication workflow begins with a two-dimensional mask layout, typically provided in GDSII or OASIS format. This layout defines the patterns that will be transferred to the wafer through lithography and subsequent processes. The virtual fabrication engine then applies a sequence of process steps, each modeled according to the underlying physics and chemistry of the actual process. As each simulated process step executes, the 3D wafer structure evolves, ultimately producing a virtual representation of the fabricated device. This 3D model enables the extraction of critical dimensions, structural profiles, material distributions, and other parameters that would traditionally require destructive cross-sectioning and advanced characterization techniques [33-35].

Fig. 1 illustrates the comprehensive virtual fabrication workflow and ecosystem. The process begins with two-dimensional layout data and process descriptions, which are transformed into detailed 3D structures through voxel-based modeling engines. Major commercial platforms, including SEMulator3D, Synopsys Process Explorer, and others, provide complementary capabilities spanning visualization, process variation analysis, yield prediction, and metrology recipe development. These platforms enable diverse applications, from gyroscope 3D structures to design verification, wafer uniformity assessment, and pattern dependence analysis, creating a comprehensive virtual development environment.

Table 1. Comparison of Commercial Virtual Fabrication Platforms

Category	Platform	Developer	Key Strengths	Primary Applications
Emulation	SEMulator3D	Coventor/Lam Research	Voxel-based 3D modeling Fast geometric simulation Advanced visualization Pattern density analysis ML/AI integration	MEMS devices Advanced packaging 3D integration Wafer-level packaging 3D NAND memory
	Process Explorer	Synopsys	Fast 3D process emulation ~1000x faster than TCAD GDSII-based modeling Quick process integration check	Advanced logic nodes DTCO workflows Design rule generation Process integration FinFET/GAA devices
Physics-based Simulation	Sentaurus Process		Physics-based dopant diffusion Advanced ion implantation Thermal/mechanical stress Calibrated equipment models	CMOS device optimization Junction engineering Well formation Oxidation/anneal Advanced logic & memory
	Victory Process	Silvaco	3D physics-based simulation Anisotropic etching models Digital Twin capability ML/AI integration	MEMS devices Power devices CMOS technology Compound semiconductors Solar cells

Physics-based modeling forms the foundation of accurate virtual fabrication. Different semiconductor processes require different modeling approaches based on their dominant physical mechanisms. Etching processes, for example, involve complex interactions between reactive species, surface chemistry, and ion bombardment. Virtual fabrication platforms typically employ phenomenological models that capture key effects, such as isotropic versus anisotropic etch behavior, aspect ratio dependent etching, microloading effects, and profile evolution [3,36]. These models incorporate parameters such as etch rates, selectivity ratios, angular dependencies, and surface reaction probabilities.

Molecular Monte Carlo simulations provide a more fundamental approach for modeling processes at the atomic and molecular scales. MC methods simulate individual particle trajectories and surface reactions, enabling the prediction of film growth, etching profiles, and material properties with high fidelity. This approach proves particularly valuable for processes where surface kinetics and stochastic effects dominate behavior. However, the computational intensity of MC simulations limits their application to relatively small simulation domains and shorter time scales compared to continuum models.

Molecular Dynamics (MD) modeling represents the most fundamental level of process simulation, directly solving Newton's equations of motion for interacting atoms. MD simulations can capture phenomena such as stress evolution during deposition, atomic mixing at interfaces, and the formation of crystallographic defects [37]. While MD provides unparalleled insights into atomic-scale mechanisms, its computational demands restrict practical applications to microscopic systems and short time scales, typically from femtoseconds to nanoseconds. Consequently, MD is often used to parameterize higher-level models rather than for full process simulation.

Table 1 provides a detailed comparison of major commercial virtual fabrication platforms, highlighting their respective strengths and target applications. SEMulator3D excels in voxel-based 3D modeling with strong visualization and virtual metrology capabilities, making it particularly suitable for MEMS and advanced packaging applications. Synopsys tools emphasize integration with electronic design automation (EDA) workflows and comprehensive lithography modeling for advanced logic nodes [21-28]. The complementary strengths of these platforms reflect the diverse requirements of modern semiconductor development, from device physics to system-level integration.

The evolution of virtual fabrication platforms reflects broader trends in semiconductor manufacturing toward increased process complexity, 3D integration, and heterogeneous systems. Modern platforms must handle not only traditional CMOS processes but also emerging technologies, including gate-all-around (GAA) transistors, 3D NAND memory, advanced packaging with through-silicon vias (TSVs) and hybrid bonding, and specialized sensor structures. This expanding scope drives the ongoing development of more accurate physical models, improved computational efficiency, and enhanced integration with design and manufacturing workflows.

3. PROCESS MODELING AND SIMULATION

Accurate modeling of individual process steps constitutes the foundation upon which virtual fabrication platforms deliver value for process development and optimization. This section examines modeling approaches for key semiconductor processes, including lithography, deposition, and etching, with a particular emphasis on challenges relevant to sensor fabrication.

3.1 Lithography Processes

Lithography represents the critical patterning step that defines device features and ultimately determines achievable dimensions in semiconductor manufacturing [15,24,28]. For sensor applications, lithography modeling must address not only conventional photoresist patterning but also specialized requirements, including thick photoresist processing for MEMS structures, multilevel metallization, and alignment accuracy for heterogeneous integration. Selection criteria for photoresist types must consider multiple factors, including target resolution, aspect ratio requirements, subsequent process steps, and sensor performance specifications. High-resolution patterning (< 1 μm) generally favors positive resists due to their superior CD control and reduced line edge roughness, which directly impact sensor sensitivity and noise characteristics. Thick film applications (> 10 μm) typically require negative resists capable of maintaining structural integrity during long development times. Process compatibility considerations include resist stability during plasma etching, wet chemical processing, and thermal cycling. Virtual fabrication of lithography processes enables the comprehensive optimization of optical proximity correction, computational lithography, and resolution enhancement techniques before committing to expensive mask fabrication and wafer processing.

The fundamental lithography workflow begins with mask design in GDSII or OASIS format, which undergoes optical proximity correction (OPC) to compensate for diffraction effects and process variations [33,34]. Virtual lithography simulation models light propagation through the optical system, photoresist exposure and development, and pattern transfer into underlying layers. Modern computational lithography incorporates sophisticated physical models, including partially coherent imaging theory, rigorous electromagnetic field simulation for sub-wavelength features, and coupled photoresist chemistry models predicting development rates as functions of local exposure dose and chemical concentrations.

For sensor fabrication, thick photoresist lithography requires specialized modeling approaches. MEMS structures often employ resist thicknesses from 10 to 100 micrometers, far exceeding standard IC photoresists. Thick resist exhibits a reduced depth of focus, pronounced standing wave effects, and complex development kinetics influenced by diffusion-limited developer penetration. Virtual fabrication models for thick resist incorporate 3D electromagnetic simulation accounting for resist topography, coupled diffusion-reaction models for development, and mechanical stress analysis predicting resist adhesion and pattern collapse.

Critical dimension (CD) uniformity control during mask manufacturing benefits from machine learning approaches combining principal component analysis (PCA), k-means clustering, and decision tree algorithms to spatially predict CD variations and enable feedforward correction to electron beam writers [28,38]. The tool signature identified through PCA enables a compensated CD residual reduction of 25%, demonstrating the value of data-driven approaches for process control.

3.2 Deposition Processes

Thin film deposition processes build up material layers with controlled thickness, composition, and properties [7,9,10,16]. Deposition modeling must address conformality, or how uniformly the deposited film coats 3D topography, as well as stress, microstructure, and interfacial properties. Different deposition processes exhibit characteristic conformality behaviors ranging from highly conformal atomic layer deposition (ALD) to directional physical vapor deposition (PVD). For sensor applications, deposition processes often require specialized materials and extreme conformality in high aspect ratio structures.

Physical vapor deposition, including evaporation and sputtering, transports material through ballistic or near-ballistic trajectories from the source to the substrate. The resulting films exhibit poor step coverage, with reduced thickness on sidewalls and in trenches. Virtual models for PVD typically employ line-of-sight deposition with sticking coefficients near unity, accurately predicting non-conformal profiles. For applications requiring gap fill or 3D structures, PVD limitations necessitate alternative deposition approaches.

Chemical vapor deposition (CVD) processes enable more conformal coverage through the surface reaction of precursor gases. The balance between the surface reaction rate and gas phase transport determines conformality. Reaction-limited CVD, where surface kinetics are slow compared to transport, produces highly conformal films. Transport-limited CVD, where reactants are rapidly consumed at exposed surfaces, yields nonconformal deposition similar to PVD. Plasma-

enhanced CVD (PECVD) introduces additional complexity through ion bombardment effects that can enhance or degrade conformality depending on process conditions.

Electroplating enables the deposition of thick metal layers for applications such as through-silicon vias, copper interconnects, and hybrid bonding pads. The electrochemical process exhibits complex behaviors influenced by current density distribution, solution chemistry, additive packages, and geometry. Virtual modeling of electroplating must capture current distribution effects that cause non-uniform thickness, including terminal effects where edges receive higher current density and deposit faster. For hybrid bonding applications, extremely flat and uniform copper surfaces are required, necessitating careful process optimization and subsequent chemical mechanical polishing [11,12].

3.3 Etching Processes

Etching represents one of the most critical and challenging processes in semiconductor fabrication, responsible for transferring patterns from photoresist masks into underlying materials [3,26,36]. The complexity of modern etching processes, particularly for high aspect ratio structures common in sensors and 3D devices, creates substantial modeling challenges. Virtual fabrication platforms must capture phenomena, including directional versus isotropic etching, aspect ratio dependent etch rates, microloading and macroloading effects, and pattern density dependencies.

Isotropic etching proceeds equally in all directions, typically dominated by the chemical reaction between etchant species and the substrate. Wet chemical etching and some plasma processes exhibit predominantly isotropic behavior. Virtual models for isotropic etching generally employ relatively simple formulations based on etch rate and time, though selectivity to different materials must be properly represented. The resulting profiles exhibit characteristic undercutting beneath mask features, with the undercut distance proportional to the etch depth.

Anisotropic etching preferentially removes material in specific crystallographic directions or shows strong directionality imposed by the etch process [29,36]. Anisotropic wet etching of silicon, for example, exhibits dramatically different etch rates on different crystal planes, enabling the fabrication of precisely controlled 3D structures. Deep reactive ion etching (DRIE) represents the most important anisotropic dry etch process for sensors and MEMS, enabling the fabrication of features with aspect ratios exceeding 100:1 [14,26,36,41]. DRIE typically employs the Bosch process, which alternates between plasma etching and sidewall passivation to achieve highly directional etching with minimal sidewall attack.

Modeling DRIE requires capturing the interplay between ion bombardment, neutral radical flux, and surface chemistry. The Bosch process parameters, including source power, bias power, pressure, gas flow rates, and cycle timing, critically determine the etch profile, surface roughness, and etch rate [36,41]. Virtual fabrication platforms typically employ phenomenological models that relate these process parameters to fundamental quantities such as ion flux, ion energy distribution, neutral flux, and sidewall passivation thickness. Calibration of these models against experimental data enables the prediction of etch profiles for new geometries and process conditions.

Aspect ratio dependent etching (ARDE) represents a particularly important phenomenon in high aspect ratio structures. As features become deeper, the flux of reactive species to the bottom decreases due to shadowing and transport limitations within the narrow opening. This leads to progressively slower etch rates as the aspect ratio increases, potentially causing an etch stop before reaching the target depth. ARDE proves especially problematic for structures with varying feature sizes, as narrower features slow down faster than wider features, creating depth non-uniformity across a pattern.

Microloading and macroloading describe pattern density effects where the etch rate depends on the local and global density of features being etched [36]. In regions with higher pattern density, the depletion of reactive species reduces the etch rate compared to isolated features. These effects create critical challenges for maintaining uniformity across complex sensor designs with varying pattern densities. Virtual fabrication enables the quantitative prediction of loading effects, facilitating design modifications or process adjustments to mitigate non-uniformity.

Fig. 2 demonstrates the complex pattern dependencies that arise in deep reactive ion etching processes. Microloading effects create etch rate variations across regions of different pattern density, with concentration distribution analysis revealing significant flux depletion in high-density areas. Aspect ratio dependent etching manifests as a progressive etch rate reduction in narrow features, potentially causing premature etch termination. Macroloading at the wafer scale produces differences between regions with varying total exposed areas. These phenomena require careful consideration in both process design and modeling, with typical Bosch process parameters spanning wide ranges of inductively coupled plasma (ICP) power, capacitively coupled plasma (CCP) bias, gas flow rates, and timing parameters to achieve desired profiles while managing these competing effects.

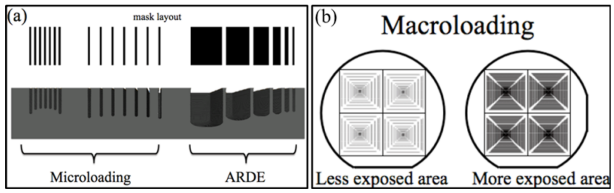

Fig. 2. DRIE process characteristics and modeling considerations; (a) Microloading effect showing concentration distribution variations between different pattern densities, ARDE effect demonstrating etch rate reduction in narrow features, (b) Macroloading effect comparing less exposed area versus more exposed area patterns, Adapted from Ref. [36].

4. CASE STUDIES AND APPLICATIONS

The practical value of virtual fabrication integrated with machine learning is best illustrated through specific applications representing diverse sensor technologies and process challenges. This section presents three case studies: the fabrication of an aluminum nitride (AlN) microcantilever actuator, wafer-level vacuum packaging for quantum sensors, and hybrid bonding for 3D integration. These examples demonstrate how virtual fabrication enables process optimization, design verification, and manufacturability assessment before committing to expensive fabrication runs.

4.1 Aluminum Nitride (AlN) Microcantilever Fabrication

Piezoelectric microcantilevers utilizing AlN thin films find applications in resonators, actuators, and biochemical sensors [29]. The fabrication process requires precise control of AlN film deposition, electrode patterning, and the sacrificial layer release to achieve the target resonant frequency, quality factor, and sensitivity. Virtual fabrication enables a comprehensive design space exploration and process optimization to maximize performance while ensuring reliable release and minimal residual stress.

The microcantilever structure consists of a multilayer stack, including the silicon substrate, a silicon dioxide sacrificial layer, a molybdenum bottom electrode, piezoelectric AlN layers, and molybdenum top electrodes [29]. Under a driving voltage U, the piezoelectric properties of the AlN film cause an additional deflection δ_p that can be related to the AlN piezoelectric coefficient d_{31} by Eq. (1), and the value of the first resonant frequency f of a three-layer bending structure can be written as follows Eq. (2) [3]:

$$\delta_p = -\frac{3}{E_{eq}h_{eq}^2}\frac{E_f(E_s h_s + E_e h_e)}{E_s h_s + E_f h_f + E_e h_e} d_{31} L^2 U \quad (1)$$

$$f_1 = \frac{p_1^2}{4\pi\sqrt{3}}\frac{h_{eq}}{L^2}\sqrt{\frac{E_{eq}}{\rho_{eq}}} \quad (2)$$

where E : Young's modulus, h : thickness, σ : stress, L : length, r : density.

The device design specifies the cantilever length, width, and thickness, along with the electrode dimensions and placement. The resonant frequency depends approximately on the ratio of frequency to length squared, with typical variations of 8% observed between the design and fabricated devices [29]. Accurate prediction of the resonant frequency requires precise knowledge of film thicknesses, densities, and elastic moduli. Moreover, the quality factor (Q-factor) serves as a key performance metric for microcantilevers and exhibits a strong dependence on fabrication process parameters through multiple energy dissipation mechanisms, making virtual fabrication particularly valuable for Q-factor optimization.

Virtual fabrication simulations begin with the deposition of the complete stack on a silicon substrate. Each layer is modeled with its actual thickness, material properties, and deposition profile. Photolithography and etching steps define the cantilever geometry and electrode patterns. The critical release process employs isotropic silicon dry etching using sulfur hexafluoride (SF_6) and oxygen (O_2) chemistry to remove the underlying silicon dioxide and silicon, leaving the cantilever suspended over a cavity.

The release etch presents multiple challenges that virtual fabrication helps address. The complete removal of sacrificial material under the full cantilever length requires sufficient etch time, but excessive etching causes a lateral undercut beyond the designed release gap. The undercut depends on the cantilever width, length, etch gap geometry, and process parameters. Virtual simulations systematically explore these dependencies, enabling optimization of design and process parameters to achieve a complete release with minimal undercut.

For a full release with low undercut, the etching process should emphasize chemical reactions over ion bombardment, achieved through high pressure, high source power, elevated gas flow rates, and minimal or zero bias power. These conditions increase the neutral radical flux while reducing the ion flux, promoting more isotropic etching that can penetrate under the cantilever. Virtual fabrication enables the quantitative prediction of the etch time required for release and the resulting undercut dimensions as functions of these process parameters.

Fig. 3 presents the AlN microcantilever structure and key considerations for the release process optimization. The multilayer stack comprises a bottom electrode, multiple

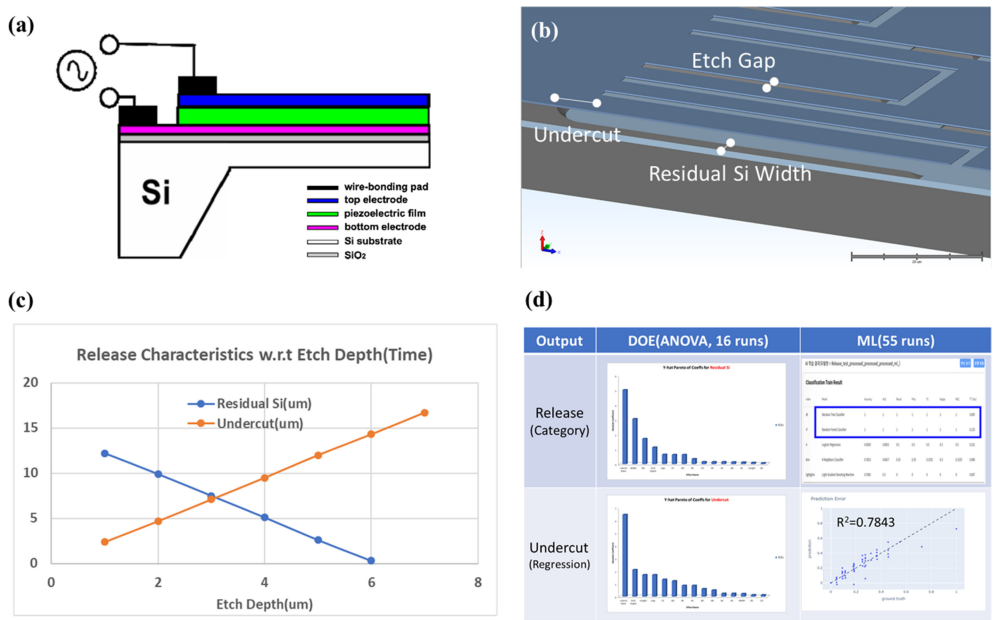

Fig. 3. AlN microcantilever parameters and virtual optimization; (a) Multilayer stack structure (PE oxide/Mo/AlN/Mo/AlN/Mo/AlN/THox/Si) showing electrode configuration, cantilever body after release, (b) 3D virtual model showing key parameters for isotropic Si dry etching including release time, undercut distance, and residual Si width as functions of cantilever width, length, and etch gap, (c) DOE (design of experiment, 16runs) results and (d) comparison with ML (machine learning, 55 runs) optimization.

piezoelectric AlN layers, and a top electrode on a silicon substrate with a silicon dioxide sacrificial layer. Critical design parameters include cantilever dimensions, etch gap geometry, and electrode placement. Virtual fabrication simulations reveal that achieving a complete release with minimal lateral undercut requires the careful balancing of process parameters to favor chemical reactions over ion bombardment. The relationship between the resonant frequency and cantilever length follows the expected quadratic dependence, with piezoelectric coefficient variations contributing to approximately 8% of the frequency variation. These simulations enable the identification of optimal design and process parameter combinations before fabrication, dramatically reducing development iterations.

The design of experiments (DOE) methodology provides a systematic sampling of the multi-dimensional parameter space. A fractional factorial design with five parameters (etch depth, lateral ratio, cantilever length, width, and gap) at two levels requires only 16 simulation runs to identify main effects and critical interactions. Analysis of variance (ANOVA) quantifies the contribution of each parameter to output metrics, including the residual silicon thickness and undercut distance.

The DOE analysis reveals that the lateral ratio and etch depth dominate the release process, accounting for over 70% of the output variation. Pareto charts visualize the relative importance of parameters, guiding the focus toward the most influential factors. The response surface methodology fits polynomial models to the simulation data, enabling the rapid prediction of release metrics across the entire parameter space without additional simulations. These surrogate models facilitate efficient optimization, identifying process conditions that achieve a complete release (residual silicon <5 μm) while minimizing the undercut (<15 μm). Complementary machine learning approaches, including neural networks, can capture more complex nonlinear relationships when warranted, though the DOE-based polynomial models prove sufficient for this application.

Experimental validation demonstrates strong agreement between virtual predictions and fabricated devices. The virtual fabrication approach reduces development time from months to weeks by eliminating numerous trial fabrication runs and enabling a confident scale-up to production.

4.2 Wafer-level Vacuum Packaging

Quantum sensors, including atomic clocks, magnetometers, and inertial sensors, often require vacuum packaging to achieve optimal performance [30]. Wafer-level vacuum packaging (WLVP) provides hermetic encapsulation with controlled cavity pressure, eliminating the need for expensive individual die-level packaging. However, the WLVP process development faces challenges, including cavity depth uniformity, seal reliability, optical transmittance for laser-based

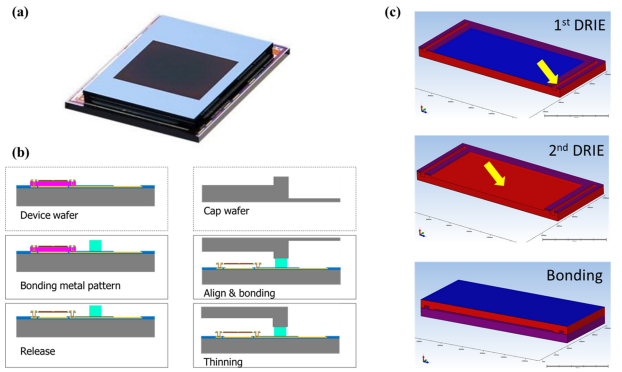

Fig. 4. Sequential DRIE process optimization for cavity wafer for WLVP; (a) Fabricated WLVP structure, (b) WLVP process for device and cavity wafer, (c) two step DRIE step and final bonding.

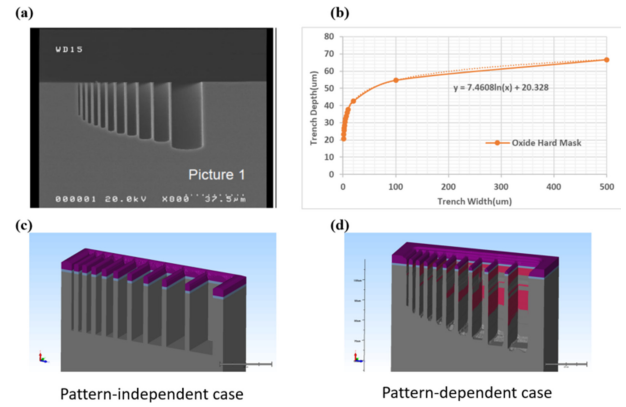

Fig. 5. Pattern dependence of DRIE for cavity wafer fabrication; (a) Experimental result, (b) Etch depth according to pattern width, (c) virtual fabrication for pattern-independent case, (d) virtual fabrication for pattern-dependent case.

sensors, and pattern density dependent etch effects.

The WLVP structure consists of a device wafer containing sensors and a cap wafer with etched cavities that house the sensors after bonding [30]. The cap wafer fabrication employs a two-step DRIE process to create the cavity structure. The first DRIE step etches completely through the wafer to define the electrical pad access. The second DRIE step partially etches through to create optical windows for light transmittance while maintaining structural support around the cavity perimeter for bonding, as shown in Fig. 4.

Pattern dependence in DRIE creates significant challenges for WLVP, as the varying feature sizes and densities across the cap wafer lead to non-uniform etch rates and depths [36]. Features smaller than approximately 100 μm exhibit a particularly strong reduction in ARDE rate, as shown in Fig. 5. Virtual fabrication enables the quantitative assessment of these pattern dependencies and the exploration of design modifications or process adjustments to improve uniformity.

Statistical optimization methods identify process parameter combinations that minimize depth non-uniformity while achieving target depths and maintaining adequate etch selectivity [13,14]. The analysis considers multiple objectives, including cavity depth uniformity, optical window thickness uniformity, and the total process time. Pareto optimization reveals fundamental trade-offs between these objectives, enabling the selection of operating points that best satisfy all requirements.

Optical transmittance through the etched windows represents another critical performance metric. Rough surfaces from DRIE scalloping degrade transmittance, particularly for thick windows [30]. Initial process conditions achieve less than 80% transmittance, which is inadequate for quantum sensor applications. Virtual fabrication coupled with optical simulation identifies that smoother sidewalls, achieved through optimized Bosch process parameters, can improve transmittance to above 90%. Machine learning models trained on virtual data enable the rapid prediction of transmittance as a function of etch parameters, facilitating efficient optimization.

The integration of cavity fabrication and bonding simulations provides end-to-end process modeling from the initial DRIE through final hermetic sealing. Virtual assessment of potential leak paths, stress concentrations, and long-term reliability informs both design and process decisions. This comprehensive modeling approach reduces development risk and accelerates the qualification of the WLVP process.

Process yield improvement represents one of the most compelling demonstrations of the virtual fabrication value. Initial experimental attempts at WLVP achieved only 30% yield due to depth non-uniformity, seal defects, and optical window breakage [30]. Virtual fabrication-guided optimization, addressing each of these failure modes, improved the yield to 100%, enabling reliable production. The cost savings from avoiding numerous failed fabrication runs and the accelerated time to production more than justify the investment in virtual process development.

4.3 Hybrid Bonding Process Optimization

Fig. 6 presents the evolution of hybrid bonding technology and its roadmap for advanced 3D integration applications [31,32]. Early adoption in Sony CMOS image sensors demonstrated the feasibility for commercial products, while high bandwidth memory (HBM) applications drove the development of fine pitch interconnection. The aggressive roadmap projects pitch scaling from the current production at several μm pitch toward a 500 nm pitch in future generations.

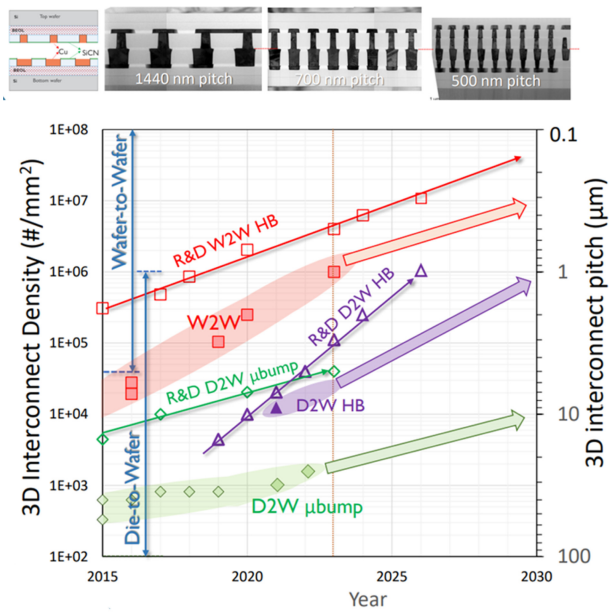

Fig. 6. HBM roadmap showing aggressive pitch scaling from 1440 nm through 1000 nm, 750 nm, to 500 nm for on-sensor AI applications, demonstrating increasing 3D interconnect density requirements. Adapted from Ref. [43].

This trajectory enables dramatically increased 3D interconnect density essential for on-sensor AI and high-performance computing applications.

The hybrid bonding process flow involves multiple critical steps, including barrier layer deposition, copper electroplating, chemical mechanical polishing (CMP), surface cleaning, wafer alignment and bonding, and post-bond annealing [11,12]. Each step must be optimized to achieve reliable bonds with low resistance and high yield. Virtual fabrication enables integrated modeling of this complete flow, identifying potential failure modes and optimizing process parameters.

Fig. 7 illustrates the critical process steps and parameters for hybrid bonding with corresponding virtual modeling approaches. Barrier layer (Ta/TaN) deposition and Cu seed layer placement require careful conformality control to ensure uniform Cu electroplating [16]. The electroplating process itself must achieve thickness uniformity across the wafer while maintaining a grain structure suitable for subsequent CMP. CMP represents the most critical step, demanding sub-nm surface roughness and minimal dishing of Cu pads relative to the surrounding oxide [11,12]. The bonding process must prevent void formation while achieving strong mechanical bonds and low electrical resistance. Experimental characterization through SEM, AFM, and TEM provides validation data, while corresponding virtual simulations enable prediction and optimization before physical experiments. This integrated experimental-virtual approach accelerates

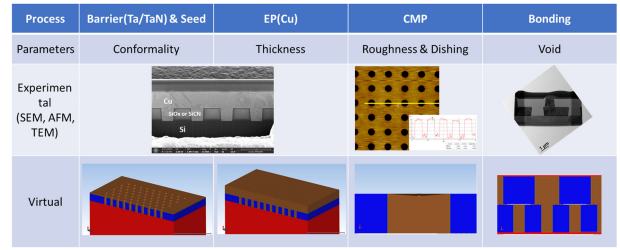

Fig. 7. Critical process steps and parameters for hybrid bonding and corresponding virtual fabrication simulations for each process step enabling prediction and optimization.

development while reducing cost and risk.

CMP represents the most critical process for hybrid bonding, as surface roughness and dishing directly impact bondability. Cu pads must be polished to achieve coplanarity with the surrounding oxide within a few nanometers while maintaining surface roughness below 1 nm RMS. Excessive dishing of Cu pads relative to the oxide prevents proper contact during bonding, while insufficient polishing leaves excess Cu that prevents oxide-oxide bonding. Virtual CMP modeling predicts dishing as a function of pad size, pattern density, and polish parameters, including time, pressure, and slurry chemistry.

Sub-micron pad bonding presents particular challenges for alignment and process windows. Misalignment between Cu pads on the two wafers can prevent electrical contact or increase resistance [32]. Virtual modeling enables the quantitative assessment of alignment tolerances and their impact on electrical performance. The simulations reveal that for pads below 1 μm in diameter, alignment tolerances must be maintained below one tenth of the pad diameter to ensure reliable contact.

The bonding process itself involves three stages: room temperature pre-bonding, intermediate temperature strengthening, and high temperature annealing [31,32]. Pre-bonding at room temperature initiates oxide-oxide bonding through hydrogen bridge formation, requiring pristine surfaces free from particles and contamination. Intermediate temperature treatment around 150-200 °C strengthens the oxide bonds. High temperature annealing above 300 °C enables copper diffusion, forming metallic bonds between the copper pads.

Virtual modeling of the bonding process incorporates multiple physical phenomena, including surface topography interaction, void nucleation and growth, Cu thermal expansion, and diffusion. Process parameters, including temperature, time, pressure, and surface condition, critically determine the bonding reliability. The design of experiments sampling across these parameters, combined with machine learning regression, enables the identification of optimal

conditions maximizing bond strength while minimizing voids and resistance [37].

Void formation represents a major failure mode in hybrid bonding, typically occurring due to trapped particles, surface roughness, or outgassing during annealing. Virtual simulations predict the probability of void formation based on surface preparation and bonding conditions. The analysis identifies critical control parameters and process windows to minimize void risk. Machine learning classification models trained on simulation data enable the rapid prediction of void risk for new process conditions.

The surface condition of the copper pad proves critical for achieving a low resistance electrical connection. Oxidation of copper surfaces during handling or cleaning can degrade bonding. Atomic simulations during plasma surface treatment can better explain the surface chemistry effects, predicting how different surface treatments and storage conditions impact final resistance. These insights guide the development of process flows that minimize copper oxidation exposure while maintaining cleanliness.

The roadmap for hybrid bonding demonstrates aggressive pitch scaling from μm-scales in current production to sub-μm in future nodes [31,32]. This scaling trajectory creates increasingly stringent requirements for alignment, surface preparation, and process control. Virtual fabrication provides an essential capability for exploring these future process regimes, identifying fundamental limits, and developing mitigation strategies before the technology nodes arrive.

5. CURRENT CHALLENGES AND FUTURE PERSPECTIVES

While virtual fabrication integrated with machine learning has demonstrated substantial value for semiconductor sensor process development, significant challenges remain that limit accuracy, scope, and adoption. Addressing these challenges while pursuing emerging opportunities will determine the trajectory of virtual process development over the coming decade. This section examines current limitations and outlines promising research directions that can advance the field toward comprehensive virtual manufacturing environments.

Multi-scale modeling complexity represents one of the fundamental challenges in virtual fabrication. Semiconductor processes involve phenomena spanning many orders of magnitude in both length and time scales. Atomic-scale processes, including surface reactions, dopant diffusion, and crystallographic defect formation, occur on angstrom and femtosecond scales. Device-scale phenomena, including film stress, thermal gradients, and electrical characteristics, span micrometers to millimeters and seconds to hours. Wafer-scale

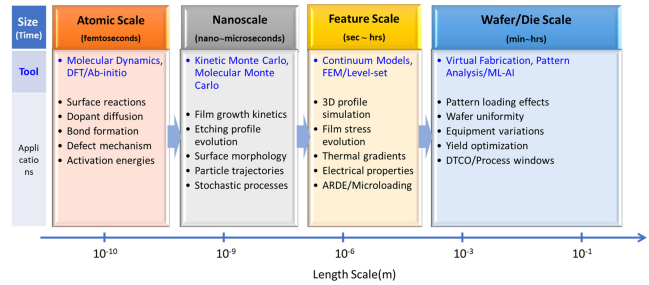

Fig. 8. Hierarchical multiscale modeling framework for semiconductor virtual fabrication spanning ten orders of magnitude in length and time scales.

effects, including pattern loading, temperature non-uniformity, and equipment variations, extend to hundreds of millimeters. Simultaneously modeling across all these scales with atomic fidelity remains computationally intractable.

Fig. 8 illustrates the hierarchical multiscale modeling framework spanning atomic-scale molecular dynamics (10^{-10} m, femtoseconds) through kinetic Monte Carlo at nanoscales (10^{-9} m, nanoseconds) to continuum finite element methods at feature scales (10^{-6} m, seconds) and virtual fabrication at wafer scales (10^{-1} m, process time).

Hierarchical multiscale modeling approaches attempt to bridge these scales by employing different levels of theory at different scales and passing information between levels [37]. Molecular dynamics simulations at the atomic scale provide parameters for kinetic Monte Carlo models at the nanoscale. Monte Carlo results inform continuum models at the device scale. However, systematic methodologies for coupling these models while maintaining accuracy and computational tractability remain active research areas. Machine learning may provide new approaches for learning effective coarse-grained models from fine-scale simulations while preserving essential physics.

Computational cost remains a practical barrier to widespread adoption of virtual fabrication despite decades of progress in computational hardware. High-fidelity 3D process simulation for a complete device with multiple process steps can require hours to days of computation even on modern workstations. For complex sensors or systems with many design variants, the computational burden becomes prohibitive. Machine learning surrogate models partially address this challenge by replacing expensive simulations with rapid predictions, but training these models still requires a substantial initial simulation effort [13,37,39].

Cloud computing and high-performance computing clusters offer scaling opportunities, enabling the parallel execution of many simulations for DOE or optimization studies. However, software licensing models, data transfer bottlenecks, and

workflow complexity often impede the effective utilization of distributed computing resources. Future virtual fabrication platforms must embrace cloud-native architectures with efficient parallelization, flexible licensing, and integrated workflow management to fully exploit available computational power.

Experimental data availability represents a critical limitation for both model calibration and machine learning training [20,30]. Accurate process models require extensive calibration data relating process parameters to experimental results for specific equipment and materials. For mature CMOS processes, decades of accumulated data and well-established PDKs provide this foundation. However, specialized sensor processes often lack comprehensive experimental databases, forcing time-consuming calibration experiments or the acceptance of reduced model accuracy.

Machine learning similarly requires substantial training data to learn accurate predictive models. While virtual fabrication can generate synthetic data through simulation, the simulations themselves must be accurate to provide value. Bootstrapping from limited experimental data to comprehensive virtual capability remains challenging. Active learning approaches that intelligently select new experiments to maximize information gain show promise for efficient data collection. Transfer learning techniques that leverage knowledge from related processes or materials may accelerate model development for new processes.

Physics-informed machine learning represents an emerging paradigm that incorporates physical knowledge into machine learning models, potentially improving data efficiency, generalization, and interpretability [37]. Rather than learning purely empirical correlations, physics-informed models embed conservation laws, symmetries, and known functional relationships. For process modeling, this might include constraints such as mass conservation during etching, diffusion equations for dopant redistribution, or stress-strain relationships for thin films. Research into physics-informed neural networks and other hybrid approaches may enable more accurate and data-efficient models.

The development of PDKs for non-standard sensor processes represents a strategic opportunity to democratize advanced fabrication technologies. Mature CMOS PDKs provide designers with comprehensive models, design rules, and characterized device libraries that enable first-time-right design. Extending this concept to MEMS, sensors, and other specialized technologies could dramatically accelerate innovation by enabling designers without deep process expertise to create manufacturable devices. Virtual fabrication provides the foundation for developing these PDKs through the systematic characterization of process capabilities, the extraction of design rules, and the generation of device libraries.

Public fabrication facility collaboration offers the potential to address the data scarcity challenge by sharing de-identified process data across organizations. University and government-sponsored fabs that support diverse research communities could contribute anonymized DOE results, process characterizations, and design libraries to shared databases. Machine learning models trained on these aggregated datasets would benefit the entire community. However, establishing appropriate data sharing frameworks, intellectual property protections, and quality standards requires careful consideration.

Artificial intelligence (AI) research collaboration can accelerate progress by connecting semiconductor domain experts with machine learning researchers developing cutting-edge algorithms. Semiconductor process optimization presents rich opportunities for advancing active learning, multi-objective optimization, physics-informed learning, and uncertainty quantification. However, much AI research focuses on different application domains, and semiconductor problems remain underrepresented in ML research. Increased collaboration through workshops, shared datasets, and joint projects could spur innovation beneficial to both communities.

6. CONCLUSIONS

This comprehensive review has examined the integration of virtual fabrication for semiconductor sensor process development, demonstrating both the substantial progress achieved and the significant opportunities ahead. Virtual fabrication platforms have matured from research tools to practical enablers of process development, providing physics-based simulation capabilities that span the full range of semiconductor unit processes. The fundamental value proposition of virtual fabrication rests on enabling informed decisions before committing to expensive physical fabrication.

For sensor applications where specialized processes often lack established design rules and comprehensive characterization, virtual fabrication provides essential capabilities for design-technology co-optimization. The case studies presented demonstrate quantifiable benefits, including a yield improvement from 30% to over 90%, a development time reduction from months to weeks, and the successful first-time fabrication of complex structures.

Critical process steps, including lithography, thin film deposition, deep reactive ion etching, chemical mechanical polishing, and hybrid bonding, all benefit from virtual modeling and optimization. For each process, virtual fabrication enables the prediction of experimental results as

functions of design parameters and process conditions, the identification of failure modes, and the optimization of process windows. The specific examples of aluminum nitride microcantilever release, wafer-level vacuum packaging with pattern-dependent DRIE, and sub-micron hybrid bonding demonstrate the breadth of applications and the depth of insights enabled.

Statistical and computational analysis tools enhance virtual fabrication by enabling the efficient exploration of multi-dimensional parameter spaces through the design of experiments, construction of response surface models for rapid prediction, and multi-objective optimization, identifying Pareto optimal solutions. These analytical approaches complement physics-based simulations, with design of experiments providing systematic parameter sampling, analysis of variance quantifying factor importance, and optimization algorithms identifying optimal operating conditions. The integration of these methods with virtual fabrication creates a powerful framework for process development that dramatically accelerates innovation while reducing cost and risk.

Current challenges, including multi-scale modeling complexity, computational cost, limited experimental data availability, and the need for comprehensive validation, remain significant. However, promising research directions, including physics-informed machine learning, digital twins, real-time process monitoring integration, and process design kit development for sensors, offer pathways to address these limitations. The convergence of advancing computational capabilities, growing experimental databases, and increasingly sophisticated machine learning algorithms points toward virtual manufacturing environments of unprecedented capability.

CRediT Authorship Contribution Statement

Joontaek Jung, Hyeonseol Kim, Jubeom Lee, Taehyun Kim: Investigation, Methodology. **Hee Yeoun Kim:** Writing – original draft, review & editing, Supervision, Funding acquisition.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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