

A D-Band Neutralized Upconversion Mixer With Enhanced Stability and Conversion Gain

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Cite This: *J. Sens. Sci. Technol.* Vol. 35, No. 5 (2026) 518-522

<https://doi.org/10.46670/JSST.2026.35.5.518>

ABSTRACT: This paper presents a 140-GHz double-balanced Gilbert-cell upconversion mixer in a 28-nm CMOS process for radar sensing and communication systems. The proposed mixer employs capacitive neutralization in the transconductance (G_m) stage and an interstage matching network between the G_m and mixing stages. The neutralization technique suppresses the feedback caused by the gate-to-drain capacitance, while the interstage matching network improves power transfer between the two stages. The mixer is designed for the RF upconversion stage of a 140-GHz D-band sliding-IF transmitter and supports a 60-GHz IF input. Simulation results show that the proposed circuit remains unconditionally stable operation over the simulated frequency range. The mixer achieves a conversion gain of 4.6 dB and an output 1-dB compression point of -5.4 dBm with a DC power consumption of 8.3 mW. Compared with the conventional Gilbert-cell architecture, the conversion gain and output 1-dB compression point are improved by approximately 3 and 1.2 dB, respectively.

KEYWORDS: D-band, Upconversion, Gilbert-cell mixer, Neutralization capacitor, Core stage matching

1. INTRODUCTION

The rapid evolution of modern sensing and communication systems has led to an increasing demand for higher sensing resolution, wider operating bandwidths, and higher data rates. In particular, emerging applications such as contactless vital-sign monitoring and integrated sensing and communication (ISAC) increasingly rely on millimeter-wave and sub-terahertz frequency bands. Among these frequency ranges, the D-band is particularly attractive for both radar sensing and high-data-rate communications, offering short wavelengths for high phase sensitivity to small target displacements and a wide available bandwidth for fine range resolution and high-capacity wireless links [1,2]. Accordingly, the design of stable and power-efficient D-band transceivers has become increasingly important for future sensing and communication systems.

In a transmitter, an upconversion mixer plays a crucial role

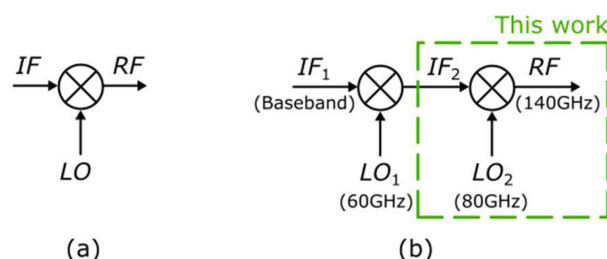


Fig. 1. Upconversion mixer. (a) Conventional architecture and (b) Sliding-IF architecture.

in translating a baseband signal to the desired radio frequency (RF) band. In a conventional transmitter architecture, the baseband signal is directly converted to the target RF frequency. However, at sub-terahertz frequencies, the generation of a high-frequency local oscillator (LO) signal becomes increasingly challenging and generally requires substantial DC power consumption, thereby degrading the overall efficiency of the transceiver. To address this limitation, a sliding-IF transmitter architecture employing multiple frequency-conversion stages was proposed in [3]. In this architecture, the LO signal is generated at a relatively low-frequency, and the desired RF signal is obtained through two frequency-conversion stages, thereby alleviating the power and implementation challenges associated with the direct generation of a sub-terahertz LO signal. The architecture

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Received : Aug. 10, 2026, Revised : Aug. 25, 2026, Accepted : Aug. 31, 2026

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shown in Fig. 1(b) is based on the same sliding-IF concept. For the frequency plan adopted in this work, a 60-GHz IF signal is generated in the first stage and mixed with an 80-GHz LO to produce the desired 140-GHz RF output, where $f_{RF} = f_{IF} + f_{LO} = 60 + 80 = 140$ GHz. Since the two LO signals are the third and fourth harmonics of a 20-GHz signal, respectively, both can be derived from a single 20-GHz VCO. In such an architecture, the second-stage upconversion mixer must process a relatively high IF signal. However, previously reported D-band upconversion mixers generally show a trade-off between high-IF operation and conversion gain or output linearity.

In this work, a Gilbert-cell-based upconversion mixer supporting a 60-GHz IF input is designed for a 140-GHz D-band sliding-IF transmitter. The proposed mixer employs a capacitive neutralization technique to mitigate the gain degradation and stability deterioration caused by the gate-to-drain capacitance (C_{GD}) of the transconductance (G_m) stage. In addition, an interstage impedance matching network is introduced between the high-frequency G_m stage and the LO-driven mixing stage to improve power transfer between the two stages and alleviate gain compression, thereby enhancing output linearity.

The remainder of this paper is organized as follows. Section II describes the conventional Gilbert-cell architecture and discusses its limitations. It then presents the proposed upconversion mixer, which mitigates these limitations through capacitive neutralization and interstage impedance matching. Section III presents the simulation results for stability, conversion gain, and linearity and compares the proposed design with the conventional architecture. Finally, Section IV summarizes the main findings and concludes this work.

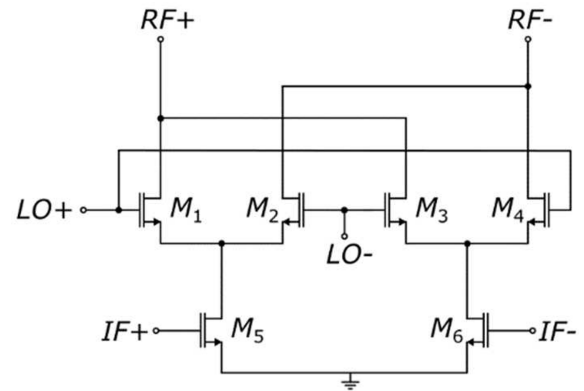


Fig. 2. Conventional Gilbert-cell mixer.

2. DESIGN OF THE PROPOSED GILBERT-CELL FREQUENCY UPCONVERTER

Fig. 2 illustrates the conventional Gilbert-cell mixer architecture. The active mixer provides conversion gain and consists of a transconductance (G_m) stage (M_5, M_6) and a mixing stage ($M_1 \sim M_4$). Owing to its circuit symmetry and high port-to-port isolation, the double-balanced architecture, in which both the input and output signals are differential, provides stable operation and suppresses undesired signal feedthrough. Although the differential mixing quad is inherently stable owing to its symmetric mixing operation, the G_m stage is structurally equivalent to a conventional common-source amplifier and therefore requires a separate stability enhancement technique. In particular, the gate-to-drain capacitance of the G_m stage transistors forms a feedback path between the input and output, which may lead to oscillation at high frequencies. Furthermore, as the operating frequency increases, signal leakage and power loss caused by the

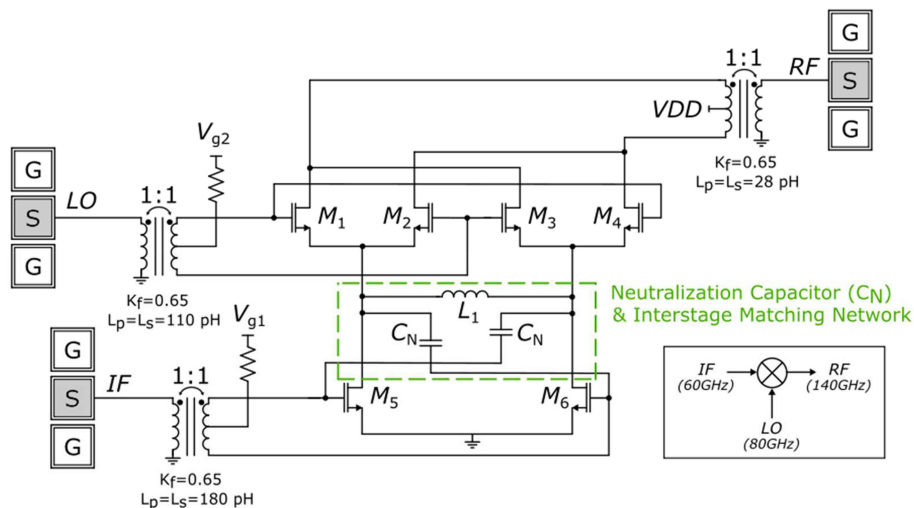


Fig. 3. Proposed architecture of upconversion mixer.

parasitic capacitance between the G_m and mixing stages become more significant. Therefore, an interstage impedance matching network is required to enhance the power transfer from the G_m stage to the mixing stage and alleviate power compression caused by impedance mismatch.

To address these two issues, this work employs a capacitive neutralization technique and an interstage impedance matching network as shown in Fig. 3. First, capacitive neutralization is applied to enhance the stability of the G_m stage [4]. As the transistor size increases, the associated parasitic capacitances also increase, and their feedback effects become more pronounced at higher frequencies, potentially resulting in positive feedback. A neutralization capacitor introduces an opposing coupling path that cancels the feedback-induced signal leakage. The resulting neutralization condition is expressed in (1) [4].

$$Y_{12} = j\omega(C_{GD} - C_x) \quad (1)$$

$$Y_{12} = g_m - j\omega(C_{GD} - C_x) \quad (2)$$

In (1) and (2), C_{GD} denotes the gate-to-drain capacitance of the transistor, whereas C_x represents the neutralization capacitance. As C_x approaches C_{GD} , the equivalent capacitance between the input and output terminals of the transistor approaches zero, thereby improving the input-to-output isolation. Consequently, the stability of the circuit is enhanced. In practice, however, the optimum C_x may differ from the nominal C_{GD} because the effective gate-to-drain capacitance is affected by layout parasitics. Therefore, C_x should be optimized at the target operating frequency to minimize the effective feedback.

Although capacitive neutralization enhances the stability of the G_m stage, impedance mismatch between the G_m and mixing stages still limits the conversion gain. Therefore, an interstage impedance matching network is employed to maximize power transfer. The real part of the interstage impedance is optimized by adjusting the transistor-size ratio between the two stages. The imaginary part is compensated using an inductor that resonates with the parasitic capacitance at the target operating frequency, thereby improving signal transfer between the G_m and mixing stages. By improving power transfer between the two stages, the matching network also mitigates gain compression and improves the output 1-dB compression point.

The input and output matching networks are implemented using transformer-based baluns at the IF, LO, and RF ports. These transformers interface the differential mixer core with single-ended 50 Ω GSG pads. At the IF and LO inputs, the transformers perform single-ended-to-differential conversion and impedance transformation for the G_m and switching stages,

respectively. The center taps of their secondary windings provide the gate-bias voltages required by the G_m and switching transistors without interfering with the differential input signals. At the RF output, the transformer combines the differential output signals and transforms the output impedance to 50 Ω . The center tap of its primary winding is connected to the DC supply voltage (VDD).

For the proposed design, the IF, LO, and RF transformers are designed with equal primary and secondary inductances ($L_p = L_s$) of 180, 110, and 28 pH, respectively, with a coupling coefficient k of 0.65 for all three transformers. These parameters are optimized at their respective operating frequencies while accounting for approximately 30 fF of device, interconnect, and pad parasitics to reduce port reflections.

3. SIMULATION RESULTS

Fig. 4 shows the simulated stability factor of the G_m stage. For the conventional Gilbert-cell architecture, the stability

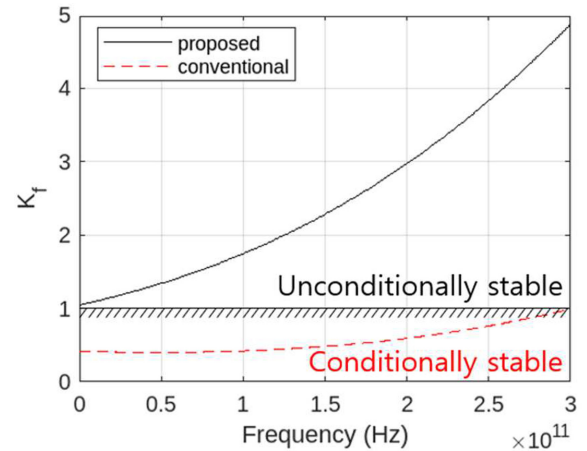


Fig. 4. Simulated results of stability.

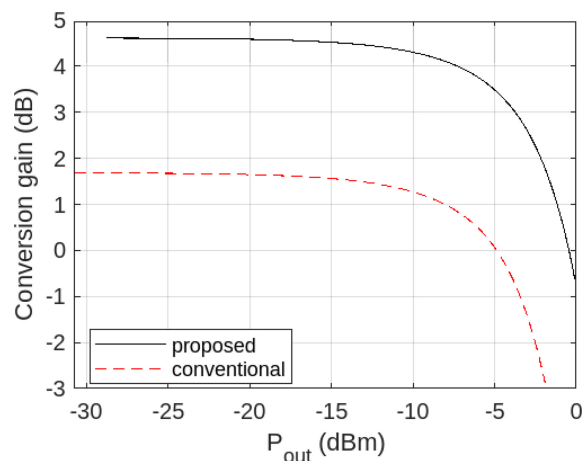


Fig. 5. Simulated linearity and conversion gain results.

Table 1. Performance Summary of D-Band Upconversion Mixers.

	This work*	[5]	[6]	[7]	[8]
Technology	28-nm CMOS	40-nm CMOS	65-nm CMOS	22-nm CMOS	55-nm CMOS
Architecture	Sliding-IF & Gilbert-cell	CG Gilbert-cell	Gilbert-cell	Gilbert-cell	High-IF & TIA-based Gilbert-cell
RF Freq. (GHz)	140	120	140	140	121.5~132.2
IF Freq. (GHz)	60	4	2.4	-	23.8~34.5
Conversion Gain (dB)	4.6	-4	7.5	1.3	-4.7
OP _{1dB} (dBm)	-5.4	-11.5	-6	1.7	-11.2
P _{DC} (mW)	8.3	9	9	5.9	8

*simulated

factor remains below unity over the entire frequency range from DC to 300 GHz and exhibits a minimum value of 0.4 at 50 GHz, indicating that the circuit may become unstable under certain source or load impedance conditions. In contrast, the proposed architecture achieves a minimum stability factor of 1.1 at DC, while maintaining a value greater than unity over the entire frequency range. These results demonstrate that the proposed circuit is unconditionally stable throughout the simulated frequency range.

Fig. 5 presents the simulated linearity and conversion gain characteristics. Under the same DC power consumption, the proposed architecture improves the output 1-dB compression point by approximately 1.2 dB and the conversion gain by approximately 3 dB compared with the conventional Gilbert-cell architecture. The proposed mixer achieves a conversion gain of 4.6 dB and an output 1-dB compression point of -5.4 dBm.

Table 1 summarizes the performance of the proposed mixer and compares it with previously reported D-band upconversion mixers. The proposed mixer supports a 60-GHz IF while maintaining DC power consumption comparable to low-IF designs ([5-7]), with competitive conversion gain and improved OP_{1dB}. It also outperforms the previously reported high-IF design ([8]) in conversion gain and output linearity.

4. CONCLUSIONS

In this work, a D-band upconversion mixer is designed in a 28-nm CMOS process to improve power transfer between the G_m and mixing stages while employing capacitive neutralization. The impedance interaction between the two stages is properly controlled through transistor sizing and inductive compensation, thereby mitigating impedance mismatch, improving power transfer, and alleviating gain compression. Meanwhile, capacitive neutralization enhances the stability of the G_m stage while further improving the conversion gain. Compared with the conventional Gilbert-cell

architecture, the proposed mixer achieves improved stability, conversion gain, and output 1-dB compression point without introducing additional active stages. These results demonstrate a simple and effective approach to enhancing D-band mixer performance with minimal circuit complexity.

CRedit Authorship Contribution Statement

Gayeong Kim: Investigation, Methodology, Validation, Visualization, Writing-original draft. **Schoon Park:** Conceptualization, Writing-review and editing, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgements

This research was supported by Kyungpook National University Research Fund, 2024.

REFERENCES

- [1] S. Park, A. Hemelhof, Y. Zhang, G. Gramegna, P. Wambacq, D-band broadband high-efficiency frequency doubler and quadrupler with optimal load impedance control in 250-nm InP DHBT, *IEEE Trans. Microw. Theory Tech.* 74 (2026) 2475–2485.
- [2] S. Park, D.-W. Park, K. Vaesen, A. Kankuppe, S. Sinha, B. van Liempd, et al., A D-band low-power and high-efficiency frequency multiply-by-9 FMCW radar transmitter in 28-nm CMOS, *IEEE J. Solid-State Circuits* 57 (2022) 2114–2129.
- [3] S.P. Singh, M.J. Nokandi, T. Rahkonen, A. Pärssinen, On the use of sub-harmonic mixer in sliding-IF architecture for mm-Wave/THz transceivers, *Proceedings of the 2nd 6G Wireless Summit (6G SUMMIT)*, Levi, Finland, 2020, pp. 1–4.
- [4] H. Asada, K. Matsushita, K. Bunsen, K. Okada, A. Matsuzawa, A 60 GHz CMOS power amplifier using

- capacitive cross-coupling neutralization with 16% PAE, Proceedings of the 6th European Microwave Integrated Circuit Conference (EuMIC), Manchester, UK, 2011, pp. 554–557.
- [5] C.J. Lee, J.-S. Kang, C.S. Park, A D-band low-power gain-boosted up-conversion mixer with low LO power in 40-nm CMOS technology, *IEEE Microw. Wireless Compon. Lett.* 27 (2017) 1113–1115.
- [6] Y. Lei, G. Su, Z. Su, X. Liu, L. Sun, A D-band up-conversion mixer with 7.5 dB gain and 40 dB LO-RF isolation in 65-nm CMOS technology, Proceedings of the 11th UK-Europe-China Workshop on Millimeter Waves and Terahertz Technologies (UCMMT), Hangzhou, China, 2018, pp. 1–3.
- [7] T. Huang, P. Hetterle, A. Engelmann, F. Probst, A.-M. Schrotz, R. Weigel, et al., A 1.7 dBm OP1dB D-band up-conversion mixer utilizing adaptive back-gate bias in 22 nm FDSOI, Proceedings of the IEEE Asia-Pacific Microwave Conference (APMC), Bali, Indonesia, 2024, pp. 525–527.
- [8] S. Yang, Analysis of high frequency behaviors of the self-biased TIA stage and implementation of an up-conversion mixer in millimeter-wave/terahertz band, *IEICE Electron. Express* 19 (2022) 20210562.